



Fast Models Fixed Virtual Platforms in Arm Development Studio

Version 11.30

Reference Guide

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This Reference Guide is written for hardware or software engineers who want to get started with the FVPs that are included in Arm Development Studio.

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1. Introduction to FVPs

Fixed Virtual Platforms (FVPs) enable software development without the need for real hardware.

They support the MTI and Iris interfaces, so can be used for debugging and for trace output. You can obtain FVPs from the following locations:

Arm® Development Studio

Includes a set of pre-built executable FVPs that are based on the following platforms:

- Base Platform
- BaseR Platform
- Arm® Versatile™ Express (VE) development boards
- Arm® MPS2 or MPS2+ platforms, for Cortex®-M series processors

For more information about Arm® Development Studio, see [Arm Development Studio Getting Started Guide](#).

Arm Architecture FVPs

Architecture Envelope Models (AEM) FVPs model Armv8-A, Armv9-A, and Armv8-R architectures.

Arm Ecosystem FVPs

Arm Ecosystem FVPs model Arm hardware subsystems targeting different market segments and applications.

Fast Models

Fast Models includes a range of FVP source code examples together with the tools needed to customize and build them. For more information, see the following links:

- [Fast Models Reference Guide](#)
- [Fast Models Tools User Guide](#)

2. Requirements for FVPs

FVPs can run on a Windows or Linux host machine.

The host has the following hardware requirements:

Architecture

FVPs support x86-64 and Arm® AArch64 host platforms.

Minimum specification

At least 2 GB RAM, preferably 4 GB.

2 GHz Intel Core2Duo, or similar, that supports the MMX, SSE, SSE2, SSE3, and SSSE3 instruction sets.

Recommended specification

At least double the RAM of the platform you intend to simulate. For example, a simulated platform containing 8 GB of DRAM should be run on a 16 GB host machine.

Fast Models and associated FVPs benefit most from high single-threaded performance. For example, a high frequency (4-5 GHz) Intel Core i9 or i7 or AMD Ryzen 9 or 7 host CPU gives a significant improvement, between 30-60%, over Intel Xeon cores (2-3 GHz).

The host has the following software requirements:

Linux

Red Hat Enterprise Linux 7 or 8 (for 64-bit architectures), Ubuntu 20.04 or 22.04 Long Term Support (LTS).

Windows

Microsoft Windows 10 64-bit.

Compiler

FVPs are built with Visual Studio 2019 and GCC 9.3.0.

3. Get started

This section describes command-line options for running the FVP from a terminal.

3.1 FVP command-line options

Specify these options when you launch an FVP from the command line. You can specify these options in any order.

Short	Long	Description
-I	--iris-server	Start Iris server allowing debuggers to connect to targets in the simulation.
-i	--iris-log	Iris log level (may be specified multiple times), example: -ii for level 2.
-A	--iris-allow-remote	Allow remote connections from other machine to Iris server (default: disabled).
	--iris-port PORT	Set a specific port to use for the Iris server.
	--iris-port-range MIN:MAX	Set the range of ports to scan when starting an Iris server. The first available port found will be used.
	--iris-connect CONSPEC	Start Iris server according to connection specification CONSPEC. Use “--iris-connect help” to get a list of supported connection types. --iris-server, --iris-allow-remote, --iris-port and --iris-port-range are ignored when using --iris-connect. Please use “--iris-connect tcpserver,allowRemote,port=X,endport=Y” to set these connection parameters.
	--cpulimit N	Number of host active CPU seconds for the simulation to run, excluding simulation startup and shutdown. Ignored when debug server started (default: unlimited).
	--cyclelimit N	Number of cycles to run, ignored when debug server started (default: unlimited).
-h	--help	Print this help message and exit.
-K	--keep-console	Keep console window open after completion (Windows only).
	--list-instances	Print list of target instances to standard output.
	--dump-instances	Write help information in JSON format to instanced_list.json and exit. Filename can be overridden by - output.
-l	--list-params	Print list of model parameters to standard output.
	--list-set-params FILE	Saves list of model parameters set and used by each component to FILE. If set to '-' print to standard output.
	--dump-params	Write help information in JSON format to parameter_list.json and exit. Filename can be overridden by - output.
	--list-regs	Print model register information to standard output.
	--list-memory	Print model memory information to standard output.
-o	--output FILE	Redirect parameters, memory and instance lists to output file FILE.
-C	--parameter SPEC	Set parameter, format: -C INST.PARAM=VALUE.
-p	--print-port-number	Print port number debug server is listening to. Use in combination with --iris-server.
-R	--run	Run the simulation immediately at start of simulation when a debug server is started. Use in combination with --iris-server.
	--stat	Print some run statistics on simulation exit.

Short	Long	Description
-T	--timelimit N	Number of wall clock seconds for the simulator to run, excluding startup and shutdown. Ignored when debug server started (default: unlimited).
-b	--break ADDRESS	Set breakpoint, format: -b [INST=][MEMSPACE@]ADDRESS (may be specified multiple times).
	--start ADDRESS	Set initial PC to application start address, format: -start [INST=]ADDRESS.
	--dump FILE@ADDRESS,SIZE	Dump section of memory into FILE, format: -dump [INST=]FILE@[MEMSPACE:]ADDRESS,SIZE (may be specified multiple times).
-q	--quiet	Run quiet, suppress informational output.
-f	--config-file FILE	Load model parameters from configuration file FILE.
	--plugin FILE	Load plugin FILE.
	--trace-plugin FILE	Load trace plugin FILE (deprecated: use -plugin).
-a	--application FILE	Application to load, format: -a [INST=]FILE (use -a INST=FILE for a specific instance, use -a INST*=FILE to match multiple instances using wildcards e.g. for SMP cores).
	--fast-ram FILE	Enable FastRAM and load the configurations of FastRAM from FILE.
	--simlimit N	Number of seconds to simulate, ignored when debug server started (default: unlimited).
	--data FILE@ADDRESS	Raw data to load at specified address, format: -data [INST=]FILE@[MEMSPACE:]ADDRESS (may be specified multiple times).
-D	--allow-debug- plugin	Allow a plugin to debug the simulation.
	--cpi-file FILE	Use FILE to set Cycle Per Instruction class.

3.2 Load code or data on the FVP

Here are the command-line options to use when loading code or data on the FVP:

-a [instance=]filename.axf

Specifies an application to load, and optionally the instance or instances to load it on. The application can be in either of the following formats, or in a gzip-compressed version:

- ELF
- Motorola S-Record

If the FVP contains multiple core instances, you can specify the instance to load the image on. The instance name can include a wildcard (*) to load the same application image into multiple cores, for example:

```
./FVP_Base_AEMvA -a cluster0.cpu*=__image.axf
```

If you omit the instance name, the application is loaded on all cores in the first cluster. If the FVP has multiple cores but no clusters, you must specify the instance name.

--data filename.bin@address

Loads binary data into memory at the address specified.

3.3 Configure the FVP

Use parameters to configure the FVP.

To display a list of all the available parameters, including a description of each one, and their default values, run the model with `--list-params`. For example:

```
./FVP_Base_AEMvA --list-params
```

Some models have many parameters. To find references to a particular feature, for example `semihosting`, on Linux, use:

```
./FVP_Base_AEMvA --list-params | grep "semihosting"
```

Or on Windows:

```
FVP_Base_AEMvA.exe --list-params | find "semihosting"
```

Specify parameters using either:

- One or more `-c` command-line arguments.
- A configuration file specified using the `-f` command-line argument.

Each `-c` command-line argument or line in the configuration file must contain:

- The name of the component instance.
- The parameter to modify.
- Its value.

Use the format:

```
instance.parameter=value
```

where `instance` can be a hierarchical path, with each level separated by a dot `.` character. For example:

```
./FVP_Base_AEMvA -C cluster0.cpu0.semihosting-enable=1 ...
```

Here, `cluster0` and `cpu0` are instance names and `semihosting-enable` is the parameter.



Note

You can set Boolean values using either `true` or `false`, or `1` or `0`.

To simplify managing multiple model parameters, specify a configuration file using the `-f` option. You can set the same parameters using this option as with the `-c` option.

Generate a configuration file with all parameters set to default values that is formatted correctly for use as input by the `-f` option by using the `-o` option. For example:

```
./FVP_Base_AEMvA --list-params -o params.cfg
```



Comment lines in the configuration file begin with a `#` character.

3.4 Debug and trace the FVP

To debug an FVP, you can either:

- Run the FVP from within an Iris-enabled debugger.
- Launch the FVP with the `-i` command-line argument. This option starts an Iris debug server which allows an Iris-enabled debugger to connect to the FVP. When `-i` is set, by default the FVP waits for the debugger to connect before it starts to run.

For information about using your debugger in these ways, see your debugger documentation. For example:

- [Iris Monitor](#)
- [Introduction to Arm Debugger](#)

All FVPs support an interface to trace events called Model Trace Interface (MTI). This interface allows FVPs to emit trace in the form of a set of trace sources. While the FVP is running, each trace source generates a stream of trace events.

Use the `--plugin` command-line argument to load a special shared object called a trace plug-in into the FVP. Trace plug-ins can consume and display trace events.

For more details about trace plug-ins, see [Plug-ins-for-Fast-Models](#).

When running an FVP, set the following environment variables to display debug messages from the simulation:

FM_SCX_VERBOSITY_LEVEL

Set to one of the following values to set the verbosity level of debug messages:

0

None

100
Low

200
Medium

300
High

400
Full

500
Debug

SCX_EVS_VERBOSE

Set to 1 to enable tracing of the default scheduler mapping implementation.

3.5 CLCD window

When an FVP starts, the CLCD window opens, representing the contents of the simulated color LCD frame buffer. It automatically resizes to match the horizontal and vertical resolution that is set in the CLCD peripheral registers.

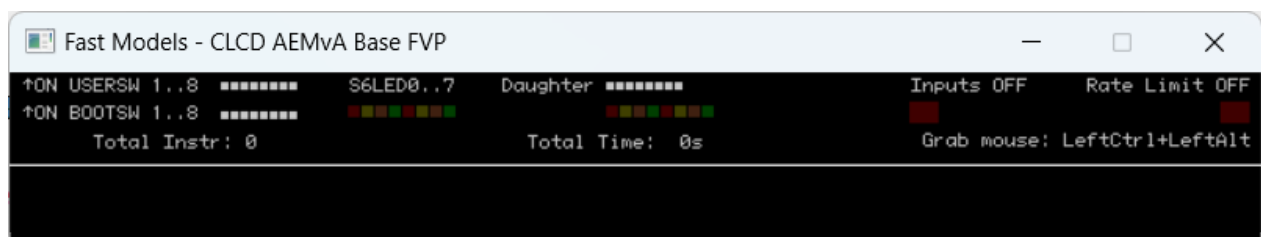
MPS2 FVPs

The LEDs and MCC switches in the CLCD window for MPS2-based FVPs correspond to the LEDs and switches on the physical board. They are controlled by the software that you load onto the FVP. For information on how to use them, see [User switches and user LEDs](#) in the MPS2 and MPS2+ FPGA Prototyping Boards TRM on Arm Developer.

Base Platform and VE FVPs

The top section of the CLCD window for Base Platform and VE FVPs displays the status information:

Figure 3-1: Base Platform CLCD window in its default state at startup

**USERSW**

Eight white boxes show the state of the User DIP switches.

These represent switch S6 on the VE hardware, USERSW[8:1], which is mapped to bits [7:0] of the SYS_SW register at address 1c010004.

The switches are in the off position by default. To change its state, click in the area above or below a white box.

BOOTSW

Eight white boxes show the state of the VE Boot DIP switches.

These represent switch S8 on the VE hardware, BOOTSEL[8:1], which is mapped to bits [15:8] of the SYS_SW register at address 1c010004 .

The switches are in the off position by default.



Changing Boot DIP switch positions while the model is running can result in unpredictable behavior.

S6LED

Eight colored boxes indicate the state of the VE User LEDs.

These represent the red/yellow/green LEDs on the VE hardware, which are mapped to bits [7:0] of the SYS_LED register at address 1c010008.

Daughter

Eight white boxes show the state of the daughterboard DIP switches and eight colored boxes show the state of the daughterboard LEDs.

Inputs

Enables or disables keyboard and mouse input capture by the running model. Input capture is enabled by default (set to ON).

Rate Limit

Enables or disables fast simulation.

Because the system model is highly optimized, your code might run faster than it would on real hardware. This effect might cause timing issues.

Rate Limit is disabled by default to favor simulation speed. Enable it to restrict simulation time so that it more closely matches real time.

To enable or disable Rate Limit, click the square button. You can also configure this option when instantiating the model with the `rate_limit-enable` visualization component parameter.

Total Instr

A counter showing the total number of instructions executed.

Because the FVP models provide a programmer's view of the system, the CLCD displays total instructions rather than total processor cycles. Timing might differ substantially from the hardware because:

- Bus fabric is simplified.
- Memory latencies are minimized.
- Cycle-approximate processor and peripheral models are used.

In general, bus transaction timing is consistent with the hardware, but the timing of operations within the model is not accurate.

Total Time

A counter showing the total elapsed time, in seconds.

This time is wall clock time, not simulated time.

When you click the `Total Instr` item in the CLCD, the display toggles to show the following:

Instr / sec

The number of instructions that execute per second of wall clock time.

Perf Index

The ratio of real time to simulation time. The larger the ratio, the faster the simulation runs. If you enable the Rate Limit feature, the Perf Index approaches unity.



You can reset the simulation counters by resetting the model.







The FVP CLCD displays the core run state for each core on each cluster using a colored icon. The icons are to the left of the `Total Instr` (or `Instr / sec`) item.

Figure 3-2: Core run state icons for a dual-cluster, quad core model



Table 3-2: Core run state icon descriptions

Icon	State label	Description
	UNKNOWN	Run status unknown, that is, simulation has not started.
	RUNNING	Core running, is not idle, and is executing instructions.

Icon	State label	Description
	HALTED	External halt signal asserted.
	STANDBY_WFE	Last instruction executed was WFE and standby mode has been entered.
	STANDBY_WFI	Last instruction executed was WFI and standby mode has been entered.
	IN_RESET	External reset signal asserted.
	DORMANT	Partial core power down.
	SHUTDOWN	Complete core power down.

If the CLCD window has focus:

- Any keyboard input is translated to PS/2 keyboard data.
- Any mouse activity over the window is translated into PS/2 relative mouse motion data. The data is then streamed to the KMI peripheral model FIFOs.



The simulator only sends relative mouse motion events to the model. As a result, the host mouse pointer does not necessarily align with the target OS mouse pointer.

You can hide the host mouse pointer by pressing the left `ctrl` + left `alt` keys. Press the keys again to redisplay the host mouse pointer. Only the left `ctrl` key is operational. The right `ctrl` key does not have the same effect.

If you prefer to use a different key, configure it with the `trap_key` visualization component parameter.

4. Base Platform

The Base Platform system model allows early development, distribution, and demonstration of software deliverables.

The standard peripheral set enables software development and porting. The platform is an evolution of the VE FVPs, which are based on the Arm® Versatile Express (VE) hardware development platform.

It provides:

- Two configurable clusters of up to eight core models that implement:
 - AArch64 at all exception levels.
 - Configurable AArch32 support at all exception levels.
 - Configurable support for little and big endian at all exception levels.
 - Generic timers.
 - Self-hosted debug.
 - Iris debug and trace.
 - GICv3 memory-mapped processor interfaces and distributor.
- Peripherals for multimedia or networking environments.
- Four PL011 UARTs.
- A CoreLink™ CCI-400 Cache Coherent Interconnect, or CCI-550 in Base Platform RevC.
- Architectural GICv3 model.
- High Definition LCD Display Controller, 1920*1080 resolution at 60fps, with single I2S and four stereo channels.
- 64MB NOR flash and board peripherals.
- CoreLink™ TZC-400 TrustZone® Address Space Controller.

4.1 Where to find software to run on a Base Platform FVP

Arm provides validated Linux and Android deliverables for FVPs.

For details, see [Getting Started with Linux or Android on Arm](#) on Arm Developer.

A software stack for running on the Armv-A Base RevC AEM FVP is provided in [GitLab](#).

Arm Development Studio has a number of example projects that target the Base Platform. For more information, see [Examples provided with Arm Development Studio](#).

4.2 Base Platform memory map

The Base Platform memory map is based on the Versatile™ Express RS2 memory map with extensions.



For an explanation of the values in the Security column, see [Base Platform secure memory](#).

Table 4-1: Base Platform memory map

Peripheral	Start address	Size	End address	Security
Trusted Boot ROM, secure flash, IntelStrataFlashJ3	0x00_0000_0000	64 MB	0x00_03FF_FFFF	S
Trusted SRAM. 512 KB is the default size. To set SRAM to 256 KB instead, set the parameter <code>bp.secure_sram_size</code> to 0.	0x00_0400_0000	512 KB	0x00_0407_FFFF	S
Trusted DRAM	0x00_0600_0000	32 MB	0x00_07FF_FFFF	S
NOR flash, flash0, IntelStrataFlashJ3	0x00_0800_0000	64 MB	0x00_0BFF_FFFF	S/NS
NOR flash, flash1, IntelStrataFlashJ3	0x00_0C00_0000	64 MB	0x00_0FFF_FFFF	S/NS
CS1-Pseudostatic RAM, PSRAM, on the motherboard.	0x00_1400_0000	64 MB	0x00_17FF_FFFF	S/NS
VRAM	0x00_1800_0000	32 MB	0x00_19FF_FFFF	S/NS
Ethernet, SMSC 91C111	0x00_1A00_0000	16 MB	0x00_1AFF_FFFF	S/NS
USB, unimplemented	0x00_1B00_0000	16 MB	0x00_1BFF_FFFF	S/NS
VE System Registers	0x00_1C01_0000	64 KB	0x00_1C01_FFFF	S/NS
System Controller, SP810	0x00_1C02_0000	64 KB	0x00_1C02_FFFF	S/NS
AACI, PL041	0x00_1C04_0000	64 KB	0x00_1C04_FFFF	S/NS
MCI, PL180	0x00_1C05_0000	64 KB	0x00_1C05_FFFF	S/NS
KMI - Keyboard, PL050	0x00_1C06_0000	64 KB	0x00_1C06_FFFF	S/NS
KMI - Mouse, PL050	0x00_1C07_0000	64 KB	0x00_1C07_FFFF	S/NS
UART0, PL011	0x00_1C09_0000	64 KB	0x00_1C09_FFFF	S/NS
UART1, PL011	0x00_1C0A_0000	64 KB	0x00_1C0A_FFFF	S/NS

Peripheral	Start address	Size	End address	Security
UART2, PL011	0x00_1C0B_0000	64 KB	0x00_1C0B_FFFF	S/NS
UART3, PL011	0x00_1C0C_0000	64 KB	0x00_1C0C_FFFF	S/NS
Watchdog, SP805	0x00_1C0F_0000	64 KB	0x00_1C0F_FFFF	S/NS
Base Platform Power Controller	0x00_1C10_0000	64 KB	0x00_1C10_FFFF	S/NS
Dual-Timer 0, SP804	0x00_1C11_0000	64 KB	0x00_1C11_FFFF	S/NS
Dual-Timer 1, SP804	0x00_1C12_0000	64 KB	0x00_1C12_FFFF	S/NS
Virtio block device	0x00_1C13_0000	64 KB	0x00_1C13_FFFF	S/NS
Virtio Plan 9 device	0x00_1C14_0000	64 KB	0x00_1C14_FFFF	S/NS
Virtio net device	0x00_1C15_0000	64 KB	0x00_1C15_FFFF	S/NS
Real-time Clock, PL031	0x00_1C17_0000	64 KB	0x00_1C17_FFFF	S/NS
CF Card, unimplemented	0x00_1C1A_0000	64 KB	0x00_1C1A_FFFF	S/NS
Color LCD Controller, PL111	0x00_1C1F_0000	64 KB	0x00_1C1F_FFFF	S/NS
VirtioRNG entropy device	0x00_1C20_0000	64 KB	0x00_1C20_FFFF	S/NS
LS64TestingFIFO	0x00_1D00_0000	64 KB	0x00_1D00_FFFF	S/NS
Utility bus for DSU-110-enabled platforms	0x00_1E00_0000	16 MB	0x00_1EFF_FFFF	NS
Non-trusted ROM, nontrustedrom	0x00_1F00_0000	4 KB	0x00_1F00_0FFF	S/NS
CoreSight™ and peripherals	0x00_2000_0000	128 MB	0x00_27FF_FFFF	S/NS
CCI-550 (Base Platform RevC only)	0x00_2A00_0000	1 MB	0x00_2A0F_FFFF	S/NS
REFCLK CNTControl, Generic Timer	0x00_2A43_0000	4 KB	0x00_2A43_0FFF	S
EL2 Generic Watchdog Control	0x00_2A44_0000	4 KB	0x00_2A44_0FFF	S/NS
EL2 Generic Watchdog Refresh	0x00_2A45_0000	4 KB	0x00_2A45_0FFF	S/NS
Trusted Watchdog, SP805	0x00_2A49_0000	64 KB	0x00_2A49_FFFF	S
TrustZone® Address Space Controller, TZC-400	0x00_2A4A_0000	4 KB	0x00_2A4A_0FFF	S
REFCLK CNTRead, Generic Timer	0x00_2A80_0000	4 KB	0x00_2A80_0FFF	S/NS
AP_REFCLK CNTCTL, Generic Timer	0x00_2A81_0000	4 KB	0x00_2A81_0FFF	S/NS
AP_REFCLK CNTBase0, Generic Timer	0x00_2A82_0000	4 KB	0x00_2A82_0FFF	S
AP_REFCLK CNTBase1, Generic Timer	0x00_2A83_0000	4 KB	0x00_2A83_0FFF	S/NS

Peripheral	Start address	Size	End address	Security
DMC-400 CFG, unimplemented	0x00_2B0A_0000	64 KB	0x00_2B0A_FFFF	S/NS
SMMUv3 AEM (Base Platform RevC only)	0x00_2B40_0000	1 MB	0x00_2B4F_FFFF	S/NS
DMA330x4 (Base Platform RevC only).	0x00_2B50_0000	1 MB	0x00_2B5F_FFFF	S/NS
GIC Physical CPU interface, GICC. To configure the address of this region use model parameters.	0x00_2C00_0000	8 KB	0x00_2C00_1FFF	S/NS
GIC Virtual Interface Control, GICH. To configure the address of this region use model parameters.	0x00_2C01_0000	8 KB	0x00_2C01_1FFF	S/NS
GIC Virtual CPU Interface, GICV. To configure the address of this region use model parameters.	0x00_2C02_F000	8 KB	0x00_2C03_0FFF	S/NS
CCI-400 (Base Platform only. RevC has a CCI-550)	0x00_2C09_0000	64 KB	0x00_2C09_FFFF	S/NS
Mali™-G76 (Base Platform RevC only)	0x00_2D00_0000	16 MB	0x00_2DFF_0000	S/NS
Non-trusted SRAM	0x00_2E00_0000	64 KB	0x00_2E00_FFFF	S/NS
GICv3 IRI GICD. To configure the address of this region use model parameters.	0x00_2F00_0000	64 KB	0x00_2F00_FFFF	S/NS
GICv3 IRI GITS. To configure the address of this region use model parameters.	0x00_2F02_0000	128 KB	0x00_2F03_FFFF	S/NS
GICv3 IRI GICR. To configure the address of this region use model parameters.	0x00_2F10_0000	1 MB	0x00_2F1F_FFFF	S/NS
PCIe config region (Base Platform RevC only)	0x00_4000_0000	256 MB	0x00_4FFF_FFFF	S/NS
PCIe memory region 1 (Base Platform RevC only)	0x00_5000_0000	256 MB	0x00_5FFF_FFFF	S/NS
Trusted Random Number Generator	0x00_7FE6_0000	4 KB	0x00_7FE6_0FFF	S
Trusted Non-volatile counters	0x00_7FE7_0000	4 KB	0x00_7FE7_0FFF	S
Trusted Root-Key Storage	0x00_7FE8_0000	4 KB	0x00_7FE8_0FFF	S
DDR3 PHY, unimplemented	0x00_7FEF_0000	64 KB	0x00_7FEF_FFFF	S/NS
HD LCD Controller, PL370	0x00_7FF6_0000	4 KB	0x00_7FF6_0FFF	S/NS
DRAM. Memory Tagging Extension (MTE) is supported.	0x00_8000_0000	2 GB	0x00_FFFF_FFFF	P
DRAM. Memory Tagging Extension (MTE) is supported.	0x08_8000_0000	30 GB	0x0F_FFFF_FFFF	P
PCIe memory region 2 (Base Platform RevC only)	0x40_0000_0000	256 GB	0x7F_FFFF_FFFF	S/NS
DRAM. Memory Tagging Extension (MTE) is supported.	0x88_0000_0000	480 GB	0xFF_FFFF_FFFF	P
DRAM. Memory Tagging Extension (MTE) is supported.	0x00_0880_0000_0000	7.5 TB	0x00_0FFF_FFFF_FFFF	P
DRAM. Memory Tagging Extension (MTE) is supported.	0x00_8800_0000_0000	120 TB	0x00_FFFF_FFFF_FFFF	P

Peripheral	Start address	Size	End address	Security
DRAM. Memory Tagging Extension (MTE) is supported.	0x08_8000_0000_0000	1920 TB	0x0F_FFFF_FFFF_FFFF	P
DRAM. Memory Tagging Extension (MTE) is supported.	0x88_0000_0000_0000	2 PB	0x8F_FFFF_FFFF_FFFF	P

4.3 Base Platform secure memory

Use the `bp.secure_memory` parameter to enable security checking on memory transactions by the TZC-400.

Table 4-2: Secure and Non-secure access permissions

Security	<code>bp.secure_memory=false</code>	<code>bp.secure_memory=true</code>
S	Secure and Non-secure access permitted.	Secure access is permitted, Non-secure access aborts.
S/NS	Secure and Non-secure access permitted.	Secure and Non-secure access permitted.
P	Secure and Non-secure access permitted.	Access conditions are programmable by the TZC-400.



Note

- The default state of the TZC-400 is to abort all accesses, even from Secure state.
- Setting both `bp.secure_memory` and `bp.has_rme` parameters to 1 is invalid and produces a warning.

Table 4-3: NSAIDs and filters that masters present to the TZC-400

Component	Non-Secure Access Identity (NSAID)	TZC-400 filter unit number (0-3)
Cluster 0	9	0
Cluster 1	9	0
VirtioNetMMIO	9	0
VirtioP9Device	8	0
VirtioBlockDevice	8	0
PL111_CLCD	7	2
HDLCD0	2	2

4.4 BaseR Platform memory map

The BaseR Platform copies its memory map from the Base Platform, but swaps the upper 2 GB of address space with the lower 2 GB.

Therefore:

- Any peripherals in the memory range `0x0` to `0x7FFFFFFF` in the Base Platform are available at the same offset in the memory range `0x80000000` to `0xFFFFFFFF` in the BaseR Platform.

- Memory in the range 0x80000000 to 0xFFFFFFFF in the Base Platform is available at the same offset in the range 0x0 to 0x7FFFFFFF in the BaseR Platform. For example, DRAM in the Base Platform memory map starts at address 0x80000000. In the BaseR Platform, this is mapped to 0.

The reason for this difference is that in the Arm®v8-R architecture, the upper 2 GB of memory does not have execution permissions by default. So, code could not run from DRAM after reset if DRAM started at address 0x80000000.

If the TCMs are enabled, for example with the parameter `-c cluster0.cpu0.tcm.a.enable=1`, then they are located at address 0. To move TCMs away from 0, use the parameters `itcm_base` and `dtcm_base`. For example:

```
-C cluster0.cpu0.itcm_base=0x8000 -C cluster0.cpu0.dtcm_base=0x18000
```

If you print the memory map of the GIC registers in a BaseR platform using the parameter `-c gic_distributor.print-memory-map=1`, the values displayed apply to the Base Platform and are incorrect for the BaseR Platform. For example:

```
GICv3 map: 0x2f000000--0x2f00ffff: GICD registers.
```

In this example, the actual address range is 0xaf000000-0xaf00ffff because in the BaseR Platform the upper and lower 2 GB address spaces are swapped.

Related information

[Base Platform memory map](#) on page 17

4.5 Base Platform DRAM

The multiple DRAM regions do not alias each other and form a contiguous 4 PB area. The total amount of DRAM on the Base Platform system model is configurable. This ability affects where usable DRAM appears.

If the Base Platform system model has `bp.dram_size=4`, the default, then 2 GB of DRAM is accessible at 0x00_8000_0000 to 0x00_FFFF_FFFF, and the remaining 2 GB is accessible at 0x08_8000_0000 to 0x08_FFFF_FFFF.

If, instead, the Base Platform system model has `bp.dram_size=8`, then 2 GB of DRAM is accessible at 0x00_8000_0000 to 0x00_FFFF_FFFF and the remaining 6 GB is accessible at 0x08_8000_0000 to 0x09_FFFF_FFFF.

The default content of RAM not otherwise written by the simulation is a repeating sequence of the 64-bit value CFDFDFDFDFDFDFCF.



Memory is allocated on demand, and performance degrades if very large amounts of memory are used.

4.6 Base Platform interrupt assignments

The platform assigns the Shared Peripheral Interrupts (SPIs) and Private Peripheral Interrupts (PPIs) on the GIC.



- SPI and PPI numbers are mapped onto GIC interrupt IDs as described in the Arm Generic Interrupt Controller Specification.
- IRQ IDs 103-111, 192-194, and 200-207 apply to the Base Platform RevC only.

Table 4-4: SPI GIC assignments

IRQ ID	SPI offset	Device
32	0	Watchdog, SP805
34	2	Dual-Timer 0, SP804
35	3	Dual-Timer 1, SP804
36	4	Real-time Clock, PL031
37	5	UART0, PL011
38	6	UART1, PL011
39	7	UART2, PL011
40	8	UART3, PL011
41	9	MCI, PL180, MCIINTRO
42	10	MCI, PL180, MCIINTR1
43	11	AACI, PL041
44	12	KMI - Keyboard, PL050
45	13	KMI - Mouse, PL050
46	14	Color LCD Controller, PL111
47	15	Ethernet, SMSC 91C111
56	24	Trusted Watchdog, SP085
57	25	AP_REFCLK, Generic Timer, CNTPSIRQ
58	26	AP_REFCLK, Generic Timer, CNTPSIRQ1
59	27	EL2 Generic Watchdog WS0
60	28	EL2 Generic Watchdog WS1
74	42	Virtio block device
75	43	Virtio P9 device
76	44	Virtio net device
78	46	VirtioRNG entropy device

IRQ ID	SPI offset	Device
80	48	TZC-400
92	60	cluster0.cpu0 PMUIRQ
93	61	cluster0.cpu1 PMUIRQ
94	62	cluster0.cpu2 PMUIRQ
95	63	cluster0.cpu3 PMUIRQ
96	64	cluster1.cpu0 PMUIRQ
97	65	cluster1.cpu1 PMUIRQ
98	66	cluster1.cpu2 PMUIRQ
99	67	cluster1.cpu3 PMUIRQ
103	71	SMMUv3 non-secure combined interrupt. Base Platform RevC only
104	72	SMMUv3 secure combined interrupt. Unused because there is no secure side. Base Platform RevC only
105	73	SMMUv3 secure event queue. Unused because there is no secure side. Base Platform RevC only
106	74	SMMUv3 non-secure event queue. Base Platform RevC only
107	75	SMMUv3 PRI queue. Unused because no PCIe device supports PRI. Base Platform RevC only
108	76	SMMUv3 secure command queue sync. Unused because there is no secure side. Base Platform RevC only
109	77	SMMUv3 non-secure command queue sync. Base Platform RevC only
110	78	SMMUv3 secure GERROR. Unused because there is no secure side. Base Platform RevC only
111	79	SMMUv3 non-secure GERROR. Base Platform RevC only
117	85	HD LCD Controller, PL370
139	107	Trusted Random Number Generator
192	160	Mali™-G76 GPU. Base Platform RevC only
193	161	Mali™-G76 GPU job. Base Platform RevC only
194	162	Mali™-G76 GPU MMU. Base Platform RevC only
200	168	PCIe INTA. Base Platform RevC only
201	169	PCIe INTB. Base Platform RevC only
202	170	PCIe INTC. Base Platform RevC only
203	171	PCIe INTD. Base Platform RevC only
207	175	PCIe SERR. Base Platform RevC only

Table 4-5: PPI GIC assignments

IRQ ID	PPI offset	Device
19	3	Secure hypervisor virtual timer interrupt
20	4	Secure hypervisor physical timer interrupt
21	5	Statistical Profiling Unit (SPU) interrupt
22	6	DCC, comms channel, interrupt
23	7	PMU, performance counter, overflow
24	8	Cross Trigger Interface (CTI) interrupt
25	9	Virtual CPU interface maintenance interrupt
26	10	Hypervisor timer interrupt
27	11	Virtual timer interrupt

IRQ ID	PPI offset	Device
28	12	Hypervisor virtual timer interrupt
29	13	Secure physical timer interrupt
30	14	Non-secure physical timer interrupt
31	15	Trace Buffer Unit (TRBU) interrupt

4.7 FVP_Base_RevC_2xAEMvA_GICv5 platform interrupt assignments

The FVP_Base_RevC_2xAEMvA_GICv5 platform is similar to FVP_Base_RevC_2xAEMvA, but with extra connections and interrupt assignments for GICv5 support.

Table 4-6: Interrupt Wire Bridge (IWB) GIC assignments

Wire number in the IWB instance	Interrupt source that connects to the IWB wire	Notes
IWB-instance-0-wire-3	Dual-Timer 1, SP804 <code>irq_out0</code> , <code>irq_out1</code>	-
IWB-instance-0-wire-42	Virtio block device	-
IWB-instance-0-wire-43	Virtio P9 device	-
IWB-instance-0-wire-44	Virtio net device	-
IWB-instance-0-wire-46	VirtioRNG entropy device	When multi IWB is enabled, VirtioRNG entropy device, <code>virtio_rng.intr</code> , is connected to IWB-instance-1-wire-0.

Table 4-7: Shared Peripheral Interrupt (SPI) GIC assignments

SPI wire	Interrupt source connecting to the SPI wire
SPI-0	Watchdog, SP805
SPI-1	Dual-Timer 0, SP804 <code>irq_out0</code> , <code>irq_out1</code>
SPI-4	Real-time Clock, PL031
SPI-5	UART0, PL011
SPI-6	UART1, PL011
SPI-7	UART2, PL011
SPI-8	UART3, PL011
SPI-9	MCI, PL180, MCIINTR0
SPI-10	MCI, PL180, MCIINTR1
SPI-11	AACI, PL041
SPI-12	KMI - Keyboard, PL050
SPI-13	KMI - Mouse, PL050
SPI-14	Color LCD Controller, PL111
SPI-15	Ethernet, SMSC 91C111

SPI wire	Interrupt source connecting to the SPI wire
SPI-24	SP805_Watchdog
SPI-25	AP_REFCLK, Generic Timer, CNTPSIRQ
SPI-26	AP_REFCLK, Generic Timer, CNTPSIRQ1
SPI-27	EL2 Generic Watchdog WS0
SPI-28	EL2 Generic Watchdog WS1
SPI-45	CCI550 async error
SPI-48	TZC-400 TrustZone interrupt signal
SPI-60	Cluster 0 PMUIRQ 0
SPI-61	Cluster 0 PMUIRQ 1
SPI-62	Cluster 0 PMUIRQ 2
SPI-63	Cluster 0 PMUIRQ 3
SPI-64	Cluster 1 PMUIRQ 0
SPI-65	Cluster 1 PMUIRQ 1
SPI-66	Cluster 1 PMUIRQ 2
SPI-67	Cluster 1 PMUIRQ 3
SPI-71	SMMUv3_FOR_PCIE comb_irpt_ns
SPI-72	SMMUv3_FOR_PCIE comb_irpt_s
SPI-73	SMMUv3_FOR_PCIE irq_out_event_queue_s
SPI-74	SMMUv3_FOR_PCIE irq_out_event_queue_ns
SPI-75	SMMUv3_FOR_PCIE irq_out_pri_queue
SPI-76	SMMUv3_FOR_PCIE irq_out_command_queue_sync_s
SPI-77	SMMUv3_FOR_PCIE irq_out_command_queue_sync_ns
SPI-78	SMMUv3_FOR_PCIE irq_out_gerror_s
SPI-79	SMMUv3_FOR_PCIE irq_out_gerror_ns
SPI-85	HD LCD Controller, PL370
SPI-107	RandomNumberGenerator
SPI-118	CCI550 event counter overflow 0
SPI-119	CCI550 event counter overflow 1
SPI-120	CCI550 event counter overflow 2
SPI-121	CCI550 event counter overflow 3
SPI-122	CCI550 event counter overflow 4
SPI-123	CCI550 event counter overflow 5
SPI-124	CCI550 event counter overflow 6
SPI-125	CCI550 event counter overflow 7
SPI-168	PCIe INTA
SPI-169	PCIe INTB
SPI-170	PCIe INTC
SPI-171	PCIe INTD
SPI-175	PCIe SERR
SPI-192	Mali™-G76 GPU

SPI wire	Interrupt source connecting to the SPI wire
SPI-193	Mali™-G76 GPU job
SPI-194	Mali™-G76 GPU MMU

4.8 Differences between Base Platform FVPs and hardware implementations

There is no hardware implementation of the Base Platform.

4.9 Base Platform startup configuration for v9 cores

Use the parameters `pctl.use_in_cluster_ppu` and `cluster.core_power_on_by_default` to configure startup of Arm®v9 cores in the Base Platform.

The following table shows the effect of each combination of these parameters:

Table 4-8: Startup behavior configuration for Armv9 cores in the Base Platform

Parameter configuration	Base Platform behavior	Recommended?
<code>pctl.use_in_cluster_ppu=true</code> <code>cluster.core_power_on_by_default=true</code>	All cores start up regardless of the PPU configuration done by the power controller. This configuration is invalid.	No
<code>pctl.use_in_cluster_ppu=false</code> <code>cluster.core_power_on_by_default=true</code>	Power controller loses the ability to do power state transitions altogether. All cores start running at once.	No
<code>pctl.use_in_cluster_ppu=true</code> <code>cluster.core_power_on_by_default=false</code>	Only cores that are mentioned in the startup quad parameter are brought up. This configuration has the limitation that the RVBAR address must be supplied as a parameter on the command line. The application start address initialized by the application loader is overridden by the reset vector address provided in the parameter.	Yes, but note the limitation described
<code>pctl.use_in_cluster_ppu=false</code> <code>cluster.core_power_on_by_default=false</code>	Wrong configuration. No core starts up.	No

4.10 Base Platform RevC

Base Platform RevC is an evolution of the Base Platform, enhanced to support exploration of system-level virtualization.

Base Platform RevC has the following additions to the Base Platform:

- A PCIeRootComplex with these address regions:
 - A PCI-E config region at 0x0040000000 to 0x004fffffffff. The PCI-E config region implements ECAM.
 - A PCI-E memory region at 0x0050000000 to 0x005fffffffff.
 - A PCI-E memory region at 0x4000000000 to 0x7fffffffff.
- An SMMUv3AEM with a control region at 0x002B400000 to 0x002B4FFFFFFF.

The SMMUv3 is placed so that accesses to memory by PCI devices acting as bus masters are affected by it.

- A DMA330x4 with a control region at 0x002B500000 to 0x002B5FFFFFFF.
- Base Platform RevC has a Corelink™ CCI-550 Cache Coherent Interconnect whereas Base Platform has a CCI-400. The CCI-550 used by RevC has a different base address for its registers (0x2A00_0000) from the base address for CCI-400 that is used by Base Platform (0x2C09_0000).
- An AHCI controller model including a SATA disk model.
- An SMMUv3TestEngine component with a control region at 0x002bfe0000 to 0x002bffFFFFFF. This component is a traffic generator that acts as a (secure) device upstream of the SMMUv3.
- Two PCIe virtio devices are above the SMMU. By default they are configured to be device 0 and 2 on bus 0.
- The PCIe devices use a DeviceID that is the same as their RequestorID (BDF).
- Base Platform RevC AEMvA FVPs include a Mali_G76 GPU.
- Base Platform RevC AEMvA FVPs implement Armv8.0 by default, which does not support the Statistical Profiling Extension (SPE). To include SPE, add parameter `cluster0.has_arm_v8-3=1`, or similar, to the command line.

Related information

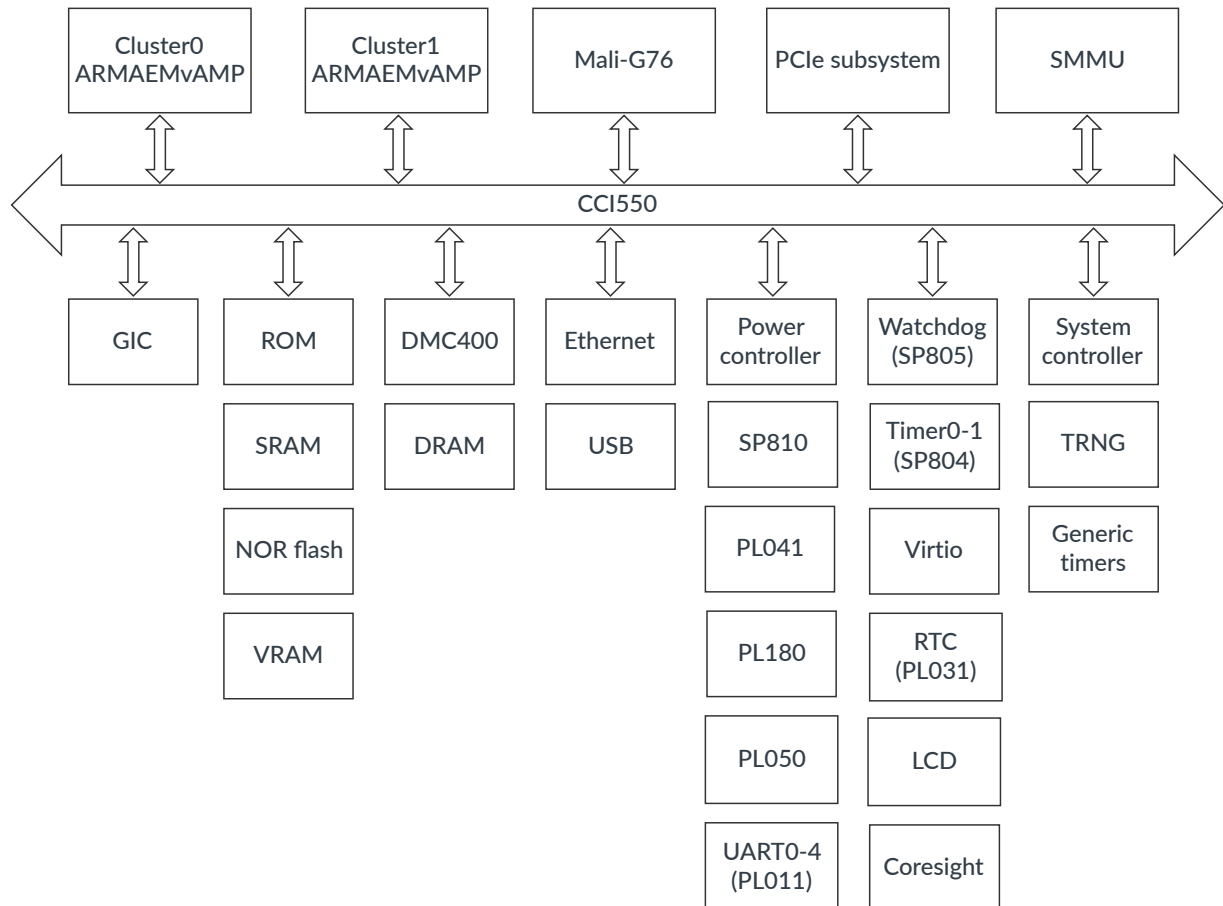
[Base Platform memory map](#) on page 17

[Base Platform interrupt assignments](#) on page 23

4.10.1 Base Platform RevC block diagram

This diagram shows the main components in Base Platform RevC. The platform shown is FVP_Base_RevC-2xAEMvA.

Figure 4-1: Base Platform RevC block diagram



4.10.2 BasePlatformPCIRevC component

This component is an integrated PCIe subsystem which forms part of the Base Platform RevC. It incorporates an SMMUv3, a PCIe, an AHCI controller, and two PCI devices which wrap a pair of virtio PCI block devices. This model is written in LISA+.



- You can include this component in a platform model, but Arm does not support using its subcomponents to create your own PCIe platform.
- The PCIe is not an implementation of any specific IP, but a functional, and limited, implementation of the PCIe standard.

BasePlatformPCIRRevC is composed of the following model components:

pci.pvbus2pci

The bridge from the Programmer's View bus to the PCI bus.

pci.pcidevice<n>

A wrapper around the underlying virtio block device. There are two block devices in the system, 0 and 1.

pci.pcivirtioblockdevice<n>

The instances of the virtio block device component.

pci.ahci_pci.ahci

An AHCI_SATA component with the following features:

- Each AHCI controller supports up to 32 simulated SATA disks. The configuration parameter `image_path` is a comma-separated list of one or more disk images.
- Supports 64-bit addresses.
- Supports plain, linear disk images, but also works with sparse files.

Some interesting options are:

- If the following options are set to non-zero values, they print messages about the operation of the bridge. The higher the value, the more verbose the component is:

```
pci.pvbus2pci.diagnostics=0x0 # (int) default = '0x0': Diagnostics level: [0x0..0x4]
pci.pcidevice<N>.diagnostics=0x0 # (int) default = '0x0': Diagnostics level:
[0x0..0x4]
```

- Each PCI device uses three BARs; one for config space, one for the MSI-X table structure and one for the MSI-X Pending Bit Array. Each of these can be configured to be 32 bits or 64 bits wide.

The Bus and Device number can be configured for each PCI device. If the device advertises MSI-X, support can be configured.

```
pci.pcidevice<N>.bus=0x0 # (int ) default = '0x0' : Bus number for this device :
[0x0..0xFF]
pci.pcidevice<N>.device=0x0 # (int ) default = '0x0' : Device number on this bus :
[0x0..0x1F]
pci.pcidevice<N>.bar0_64bit=0 # (bool) default = '0' : If BAR 0 is 64 bits wide, if
region size is nonzero
pci.pcidevice<N>.msix_support=0 # (bool) default = '0' : Enable device support for
MSI-X
pci.pcidevice<N>.bar2_64bit=0 # (bool) default = '0' : If BAR 2 is 64 bits wide, if
region size is nonzero
pci.pcidevice<N>.bar4_64bit=0 # (bool) default = '0' : If BAR 4 is 64 bits wide, if
region size is nonzero
```

- The following option configures the image file that the virtio block device exposes:

```
pci.pcivirtioblockdevice<N>.image_path="" # (string) default = '' : image file path
```

- There are two `PVBusLogger`s in the `pdbus2pci` component. One is in front of the Configuration space and one is in front of the Device space:

```
FVP_Base_AEMvA_AEMvA-PCI.pci.pvbus2pci.devicellogger
FVP_Base_AEMvA_AEMvA-PCI.pci.pvbus2pci.cfglogger
```

- There is one `PVBusLogger` in the `pcidevice` component. This reports on DMA accesses by the PCI device:

```
FVP_Base_AEMvA_AEMvA-PCI.pci.pcidevice0.dmalogger
```

- There is a `PVBusLogger` downstream of the SMMU. This reports on the transactions after they have been transformed by the SMMU:

```
FVP_Base_AEMvA_AEMvA-PCI.pci.smmullogger
```

Use the [GenericTrace](#) plug-in to capture traces from the loggers. For example, to see all accesses to device space, add the following options to the command line:

```
--plugin GenericTrace.so
-C TRACE.GenericTrace.trace-sources="FVP_Base_AEMvA_AEMvA-PCI.pci.pvbus2pci.devicellogger.*"
```

Use the [ListTraceSources](#) plug-in to list all the available trace sources in the model.

- To supply the AHCI controller with one or more SATA disk images, use the `image_path` parameter. For example:

```
-C pci.ahci_pci.ahci.image_path=disk1tb.img,disk8tb.img
```

Table 4-9: BasePlatformPCIRevC ports

Name	Protocol	Type	Description
<code>smmu_incoming_pvbus_s</code>	PVBus	Slave	Input port to smmu incoming device traffic slave based on PVBus protocol.
<code>pdbus_address_map_s</code>	PVBus	Slave	Input port to service transactions based on the PVBus protocol.
<code>pdbus_address_map_m</code>	PVBus	Master	Output port to send out PVBus transactions that are not handled by this component.
<code>system_reset</code>	Signal	Slave	Input port to handle reset signals. It is used to reset the internal state of this component.
<code>sev_out</code>	Signal	Peer	Port to send out a notification of the occurrence of an event as <code>sg::Signal</code> to a peer.
<code>interrupts[224]</code>	Signal	Master	Array of output ports of type <code>sg::Signal</code> to send out interrupts generated by this component.
<code>pdbus_pci_dma_m</code>	PVBus	Master	Output port to send out any DMA (of PVBus protocol) accesses originating from this component.
<code>clk_in</code>	ClockSignal	Slave	Input port to connect to a ClockSignal provider.

Table 4-10: BasePlatformPCIRRevC parameters

Name	Type	Allowed values	Default value	Description
ITS0-base	uint64_t	0 - 0xFFFFFFFFFFFFFFFF	0x2f020000	The ITS0 Base address.
pci_smmuv3. mmu.SMMU_IDR1	uint32_t	0 - 0xFFFFFFFF	0xe739d10	SMMU_IDR1.
pci_smmuv3. mmu.smmu_ msi_device_id	uint32_t	0 - 0xFFFFFFFF	0x10000	When appropriately enabled, assume that MSIs that are generated by the SMMU are presented to the GIC with this DeviceID. See parameters <code>msi_attribute_transform</code> and <code>enable_device_id_checks</code> .

Related information

[SMMUv3AEM](#)

[VirtioBlockDevice](#)

4.10.3 Base Platform RevC PCIeRootComplex

This component is an abstraction that represents the root of a PCIe device tree.

The addressable regions are also available as the following model parameters:

- PCIE_CFG_START, PCIE_CFG_END
- PCIE_MEM0_START, PCIE_MEM0_END
- PCIE_MEM1_START, PCIE_MEM1_END

PCIe device types:

Bridge

For example Root Port, Switch.

Endpoint

For example AHCI_SATA, SMMUv3TestEngine.

The PCIe device tree has the following properties:

- It always has PCIeRootComplex (RC) as its root.
- RC can connect to a Bridge or to an EndPoint.

PCIe device tree specification:

- The entire PCIe device tree can be specified through the model parameter `hierarchy_file_name` whose format is JSON. If no file is supplied, a default tree is assumed.

- Start the model and use the MTI trace source `ROOT_COMPLEX_HIERARCHY` to see the exact tree and parameter used for each device in the default tree. For example:

```
-C TRACE.GenericTrace.trace-  
sources="FVP_Base_RevC_2xAEMvA.pci.pcie_rc.ROOT_COMPLEX_HIERARCHY"
```

- The top-level devices of the default tree are: AHCI_SATA, HostBridge, ROOTPORT0, ROOTPORT1, ROOTPORT2, ROOTPORT3, SMMUv3TestEngine0, SMMUv3TestEngine1. ROOTPORT1-4 are of type `PCIEBridge` with parameter `port_type = 4`.

Error responses from PCIe devices:

- AMBA SLVERR (TX_ABORT) to PCIe Completer Abort (CA)
- AMBA DECERR (TX_DECODEABORT) to PCIe Unsupported Request (UR)

4.10.4 Base Platform RevC SMMUv3AEM

This is an architectural model implementing the SMMUv3.0 and SMMUv3.1 architectures which are for I/O virtualization of devices. The SMMU is placed so that accesses to memory by PCI devices acting as bus masters are affected by it.

The SMMU has the following features:

- Memory that is mapped to the range `0x2B400000-0x2B4FFFFFF`.
- Interrupts with IRQ IDs in the range 103-111.
- The event output pin of the SMMU is passed to the clusters.
- The downstream ports of the SMMU attach to the coherent bus infrastructure and so are coherent with the core clusters. All cores and the SMMU are in the same shareability domain. There is no distinction between the inner and outer shareability domains.
- The parameters of the SMMU determine its capabilities and have default values which can be overwritten if necessary.
- The SMMU is configured to only accept 16-bit StreamIDs and there is a 1:1 correspondence between RequestorID and StreamID.
- By default, the SMMU uses DeviceID `0x10000` to identify itself to the GIC (`pci.pci_smmuv3.mmu.smmu_msi_device_id`).

The parameter `gic_distributor.ITS-device-bits` is set to 17 by default to support the 17-bit DeviceIDs.

The SMMU has the following limitations:

- It does not support RAS.
- The PMU has limited functionality. Only a subset of the architecturally mandatory events are supported, as indicated by the `SMMU_PMC_CCEID0` fields. The PMU is intended for demonstration purposes only and for driver development.

4.10.5 Base Platform RevC PCIe device assignment

Every PCIe Endpoint can be enabled to support this feature which makes the Endpoint assignable to a Trusted Compute Base (TCB).

When an Endpoint is assigned to a TCB, it can be configured to both handle and generate memory transactions to specific memory regions.

The model has the following features:

- DOE read/write mailbox.
- SPDМ messages including FINISH_RESPONSE. There is no encryption of messages yet.
- IDE capability on device and root-port.
- Secure-SPDM. There is no MAC, encryption.
- TDISP messages and state machine.

To enable the device assignment feature in a PCIe RootPort, use the `rootportda_supported` parameter. To enable the feature in a PCIe Endpoint, use the following parameters:

doe_supported

Enables the PCIe extended capability called Data Object Exchange.

ide_supported

Enables the PCIe extended capability called Integrity and Data Encryption. This parameter also exists on the PCIe RootPort. The FVP does not model any encryption details but responds appropriately for “IDE” request messages.

x509_cert_der_filename

Filename containing an X-509 certificate issued for this DOE device in DER format. This certificate should contain the corresponding public key of the pair containing parameter `<rsa_priv_key_pem_filename>`.

rsa_priv_key_pem_filename

Filename containing a RSA private key, in PEM, for this DOE device. The corresponding RSA public key should be used to create parameter `<x509_cert_der_filename>`.

dmtf_meas_spec_info

Information about the DMTF measurement specification format. See the DMTF measurement specification format table for more information. Use the following format for the content of each line in this file:

`index_num_in_dec,dmtf_meas_spec_value_type,measurement_filename`

For example:

```
0,8,meas1.txt
1,9,meas2.txt
10,0,meas3.txt
```

4.10.6 Base Platform RevC legacy PCI interrupts

Each PCI device is hardwired to use INTA, with a value of 1 in the `interrupt_pin` register. This is required by the PCI specification for single-function devices.

The interrupts in the PCI host bridge are mapped according to section 2.2.6 of the PCI Local Bus Specification Revision 3.0, using the following formula, where the values for DeviceInterrupt are INTA = 0, INTB = 1, INTC = 2, INTD = 3:

```
BridgeInterrupt = (Device + DeviceInterrupt) % 4
```

This formula produces the following mappings:

Table 4-11: Mapping BridgeInterrupts to DeviceInterrupts

BridgeInterrupt ID	DeviceInterrupt
200	INTA
201	INTB
202	INTC
203	INTD
207	SERR

4.10.7 Base Platform RevC MSI-X

The model optionally implements MSI-X, depending on whether the parameter `msix_support` is set. If set, an MSI-X capability is advertised as a PCI capability.



Note

The Virtio specification is not fully compliant with the PCI specification and the virtio block device cannot be used in a 'pure polling' mode where MSI-X is always masked and only polling the Pending Bit Array is used.

The MSIs produced by the models, when directed to the GIC, have their payload rewritten to carry the DeviceID of the originating device to the GIC.

4.11 Base Platform clocks

This table shows the clock frequencies of the Base Platform peripherals.

Table 4-12: Peripheral clock frequencies in the Base Platform

Device	Clock
Clusters	100 MHz
REFCLK CNTControl, Generic Timer	100 MHz

Device	Clock
AP_REFCLK CNTCTL, Generic Timer	100 MHz
Dual-Timer 0-1, SP804	35 MHz
VE system registers	24 MHz
UART 0-3, PL011	24 MHz
KMI 0-1, PL050	24 MHz
MCI, PL180	24 MHz
AACI, PL041	24 MHz
Ethernet, SMSC 91C111	24 MHz
Watchdog, SP805	24 MHz
Color LCD Controller, PL111	23.75 MHz
HD LCD Controller, PL370	10 MHz
Trusted Watchdog, SP805	32.768 kHz
Real-time Clock, PL031	1 Hz

4.12 Base Platform FVPs

This section lists the instances in each FVP.

4.12.1 Instances for FVP_Base_AEMvA

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_AEM-A_MP](#)
- [AudioOut_SDL](#)
- BasePlatformPeripherals
- [Base_PowerController](#)
- CCI400
- ClockDivider
- ClockTimerThread
- ClockTimerThread64
- Cluster_ARM_AEM-A_MP
- CounterModule
- DebugAccessPort
- DebugROM
- ElfLoader
- FVP_Base_AEMvA

- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)

- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.2 Instances for FVP_Base_C1-Nano

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_C1-Nano](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_C1-Nano](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)

- FVP_Base_C1_Nano
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMCU

- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.3 Instances for FVP_Base_C1-Premium

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_C1-Premium](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_C1-Premium](#)
- [CounterModule](#)
- [DebugAccessPort](#)

- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_C1_Premium](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)

- [RootKeyStorage](#)
- [SMCU](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.4 Instances for FVP_Base_C1-Pro

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_C1-Pro](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_C1-Pro](#)

- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_C1_Pro](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)

- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMCU](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.5 Instances for FVP_Base_C1-Ultra

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_C1-Ultra](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)

- [ClockTimerThread64](#)
- [Cluster_ARM_C1-Ultra](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_C1_Ultra](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)

- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMCU](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.6 Instances for FVP_Base_Cortex-A32

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A32](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)

- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A32](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A32](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)

- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.7 Instances for FVP_Base_Cortex-A320

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A320](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)

- CCI400
- ClockDivider
- ClockTimerThread
- ClockTimerThread64
- Cluster_ARM_Cortex-A320
- CounterModule
- DebugAccessPort
- DebugROM
- ElfLoader
- FVP_Base_Cortex_A320
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse

- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.8 Instances for FVP_Base_Cortex-A34

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A34](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)

- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A34](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A34](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)

- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.9 Instances for FVP_Base_Cortex-A35

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A35](#)
- [AudioOut_SDL](#)

- BasePlatformPeripherals
- Base_PowerController
- CCI400
- ClockDivider
- ClockTimerThread
- ClockTimerThread64
- Cluster_ARM_Cortex-A35
- CounterModule
- DebugAccessPort
- DebugROM
- ElfLoader
- FVP_Base_Cortex_A35
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD

- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.10 Instances for FVP_Base_Cortex-A510

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A510](#)

- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A510](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A510](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)

- [PL370_HDLCDC](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.11 Instances for FVP_Base_Cortex-A520

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A520](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A520](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A520](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)

- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.12 Instances for FVP_Base_Cortex-A520AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A520AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A520AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A520AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)

- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)

- [v8ECT_Component](#)

4.12.13 Instances for FVP_Base_Cortex-A53

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A53](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A53](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A53](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)

- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)

- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.14 Instances for FVP_Base_Cortex-A55

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A55](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A55](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A55](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)

- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)

- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.15 Instances for FVP_Base_Cortex-A57

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A57](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A57](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A57](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)

- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)

- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.16 Instances for FVP_Base_Cortex-A65

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A65](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A65](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A65](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)

- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)

- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.17 Instances for FVP_Base_Cortex-A65AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A65AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A65AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A65AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)

- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)

- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.18 Instances for FVP_Base_Cortex-A710

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A710](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A710](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A710](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)

- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)

- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.19 Instances for FVP_Base_Cortex-A715

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A715](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A715](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A715](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)

- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)

- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.20 Instances for FVP_Base_Cortex-A72

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A72](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A72](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A72](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)

- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)

- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.21 Instances for FVP_Base_Cortex-A720

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A720](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A720](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A720](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)

- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMSC_91C111
- SP804_Timer
- SP805_Watchdog
- SP810_SysCtrl
- SchedulerThread
- SchedulerThreadEvent
- TLB
- TZC_400
- TelnetTerminal

- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.22 Instances for FVP_Base_Cortex-A720AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A720AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A720AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A720AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)

- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)

- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.23 Instances for FVP_Base_Cortex-A725

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A725](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A725](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A725](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)

- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)

- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.24 Instances for FVP_Base_Cortex-A73

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A73](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A73](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A73](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)

- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMSC_91C111
- SP804_Timer
- SP805_Watchdog
- SP810_SysCtrl
- SchedulerThread
- SchedulerThreadEvent

- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.25 Instances for FVP_Base_Cortex-A75

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A75](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A75](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A75](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)

- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)

- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.26 Instances for FVP_Base_Cortex-A76

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A76](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A76](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A76](#)
- [FlashLoader](#)
- [GIC_IRI](#)

- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMSC_91C111
- SP804_Timer
- SP805_Watchdog
- SP810_SysCtrl

- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.27 Instances for FVP_Base_Cortex-A76AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A76AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A76AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A76AE](#)
- [FlashLoader](#)

- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)

- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.28 Instances for FVP_Base_Cortex-A77

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A77](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A77](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A77](#)

- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)

- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.29 Instances for FVP_Base_Cortex-A78

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A78](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A78](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)

- FVP_Base_Cortex_A78
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMSC_91C111

- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.30 Instances for FVP_Base_Cortex-A78AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A78AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A78AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)

- [ElfLoader](#)
- [FVP_Base_Cortex_A78AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)

- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.31 Instances for FVP_Base_Cortex-A78C

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-A78C](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-A78C](#)
- [CounterModule](#)
- [DebugAccessPort](#)

- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_A78C](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)

- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.32 Instances for FVP_Base_Cortex-X1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X1](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-X1](#)
- [CounterModule](#)

- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X1](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)

- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.33 Instances for FVP_Base_Cortex-X1C

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X1C](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-X1C](#)

- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X1C](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)

- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.34 Instances for FVP_Base_Cortex-X2

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X2](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)

- [Cluster_ARM_Cortex-X2](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X2](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)

- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.35 Instances for FVP_Base_Cortex-X3

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X3](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)

- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-X3](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X3](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)

- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.36 Instances for FVP_Base_Cortex-X4

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X4](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)

- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-X4](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X4](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)

- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.37 Instances for FVP_Base_Cortex-X925

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-X925](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)

- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-X925](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Cortex_X925](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)

- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.38 Instances for FVP_Base_Neoverse-E1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-E1](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)

- CCI400
- ClockDivider
- ClockTimerThread
- ClockTimerThread64
- Cluster_ARM_Neoverse-E1
- CounterModule
- DebugAccessPort
- DebugROM
- ElfLoader
- FVP_Base_Neoverse_E1
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse

- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.39 Instances for FVP_Base_Neoverse-N1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-N1](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)

- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-N1](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_N1](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)

- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.40 Instances for FVP_Base_Neoverse-N2

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-N2](#)
- [AudioOut_SDL](#)

- BasePlatformPeripherals
- Base_PowerController
- CCI400
- ClockDivider
- ClockTimerThread
- ClockTimerThread64
- Cluster_ARM_Neoverse-N2
- CounterModule
- DebugAccessPort
- DebugROM
- ElfLoader
- FVP_Base_Neoverse_N2
- FlashLoader
- GIC_IRI
- GUIPoll
- HostBridge
- IntelStrataFlashJ3
- LS64TestingFIFO
- Labeller
- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD

- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.41 Instances for FVP_Base_Neoverse-N3

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-N3](#)

- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-N3](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_N3](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)

- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.42 Instances for FVP_Base_Neoverse-V1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-V1](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-V1](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_V1](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)

- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.43 Instances for FVP_Base_Neoverse-V2

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-V2](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-V2](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_V2](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)

- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)

- [v8ECT_Component](#)

4.12.44 Instances for FVP_Base_Neoverse-V3

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-V3](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-V3](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_V3](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)

- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)

- [WarningMemory](#)
- [v8ECT_Component](#)

4.12.45 Instances for FVP_Base_Neoverse-V3AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Neoverse-V3AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Neoverse-V3AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_Base_Neoverse_V3AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)

- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)

- [VisEventRecorder](#)
- [WarningMemory](#)
- [v8ECT_Component](#)

4.13 BaseR Platform FVPs

This section lists the instances in each FVP.

4.13.1 Instances for FVP_BaseR_AEMv8R

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARMAEMv8-R_MP](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARMAEMv8-R_MP](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_BaseR_AEMv8R](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)

- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)

- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [gic_iri](#)
- [v8ECT_Component](#)

4.13.2 Instances for FVP_BaseR_Cortex-R52

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_CortexR52](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R52](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_BaseR_Cortex_R52](#)
- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)

- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TelnetTerminal](#)
- [VEDCC](#)

- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [gic_iri](#)
- [v8ECT_Component](#)

4.13.3 Instances for FVP_BaseR_Cortex-R52Plus

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R52Plus](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R52Plus](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_BaseR_Cortex_R52Plus](#)
- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)

- MMC
- MemoryMappedCounterModule
- MemoryMappedGenericTimer
- MemoryMappedGenericWatchdog
- NonVolatileCounter
- OrGate
- PASSwitch
- PL011_Uart
- PL031_RTC
- PL041_AACI
- PL050_KMI
- PL111_CLCD
- PL11x_CLCD
- PL180_MCI
- PL370_HDLCD
- PS2Keyboard
- PS2Mouse
- PVBusExclusiveMonitor
- PVBusLogger
- PVCache
- PVMemoryProtectionEngine
- PVMetadataController
- RAMDevice
- RandomNumberGenerator
- RootKeyStorage
- SMSC_91C111
- SP804_Timer
- SP805_Watchdog
- SP810_SysCtrl
- SchedulerThread
- SchedulerThreadEvent
- TLB
- TZC_400
- TelnetTerminal

- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [gic_iri](#)
- [v8ECT_Component](#)

4.13.4 Instances for FVP_BaseR_Cortex-R82

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R82](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R82](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_BaseR_Cortex_R82](#)
- [FlashLoader](#)
- [GIC_IRI](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)

- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)

- [TZC_400](#)
- [TZSwitch](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [gic_iri](#)
- [v8ECT_Component](#)

4.13.5 Instances for FVP_BaseR_Cortex-R82AE

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R82AE](#)
- [AudioOut_SDL](#)
- [BasePlatformPeripherals](#)
- [Base_PowerController](#)
- [CCI400](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R82AE](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- [DebugROM](#)
- [ElfLoader](#)
- [FVP_BaseR_Cortex_R82AE](#)
- [FlashLoader](#)
- [GIC_IRI](#)

- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [LS64TestingFIFO](#)
- [Labeller](#)
- [MMC](#)
- [MemoryMappedCounterModule](#)
- [MemoryMappedGenericTimer](#)
- [MemoryMappedGenericWatchdog](#)
- [NonVolatileCounter](#)
- [OrGate](#)
- [PASSwitch](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL370_HDLCD](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVBusLogger](#)
- [PVCache](#)
- [PVMemoryProtectionEngine](#)
- [PVMetadataController](#)
- [RAMDevice](#)
- [RandomNumberGenerator](#)
- [RootKeyStorage](#)
- [SBIST_Controller](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)

- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TLB](#)
- [TZC_400](#)
- [TZSwitch](#)
- [TelnetTerminal](#)
- [VEDCC](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VirtioBlockMMIO](#)
- [VirtioEntropyMMIO](#)
- [VirtioNetMMIO](#)
- [VirtioP9Device](#)
- [VisEventRecorder](#)
- [WarningMemory](#)
- [gic_iri](#)
- [v8ECT_Component](#)

5. MPS2

The Microcontroller Prototyping System 2 (MPS2) Fixed Virtual Platforms (FVPs) implement a subset of the functionality of the Arm Versatile Express V2M-MPS2 and V2M-MPS2+ motherboard hardware.

MPS2 platforms include MPS2-specific components and generic components, such as buses and timers. They are sufficiently accurate to boot the Keil RTX RTOS and run the Blinky application.

5.1 MPS2 memory map for models without the Armv8-M additions

This section describes the MPS2 memory map for older cores, without the Armv8-M additions.

For standard Arm peripherals, see the TRM for that device.



- A bus error is generated for accesses to memory areas not shown in this table.
- Any memory device that does not occupy the total region is aliased within that region.

Table 5-1: Memory map for models without the Armv8-M additions

Description	Modeled	Address range
Ethernet. Through ahb_to_extmem16. Offset 0x0 to 0x0FE for CSRs, 0x100 to 0x1FE for FIFO.	Partial	0xA0000000 to 0xA000FFFF
PSRAM (16 MB)	Yes	0x60000000 to 0x60FFFFFF
VGA Image (512x128) (AHB)	Yes	0x41100000 to 0x4110FFFF
VGA Console (AHB)	Yes	0x41000000 to 0x4100FFFF
Block RAM (boot time). Reserved 64 KB, 16 KB implemented. This memory is wrapped through the region.	Yes	0x40200000 to 0x402FFFFFF
Reserved	N/A	0x40030000 to 0x401FFFFFF
SCC register	Yes	0x4002F000 to 0x4002FFFF
Reserved	N/A	0x40029000 to 0x4002EFFF
FPGA System Control & I/O, APB	Yes	0x40028000 to 0x40028FFF
Reserved	N/A	0x40025000 to 0x40027FFF

Description	Modeled	Address range
Audio I2S, APB	Partial	0x40024000 to 0x40024FFF
SBCon (Audio Configuration), APB	Yes	0x40023000 to 0x40023FFF
SBCon (Touch for LCD module), APB	Partial	0x40022000 to 0x40022FFF
PL022 (SPI for LCD module), APB	Partial	0x40021000 to 0x40021FFF
PL022 (SPI), APB	Yes	0x40020000 to 0x40020FFF
CMSDK system controller	Yes	0x4001F000 to 0x4001FFFF
Reserved for extra GPIO & other AHB peripherals	N/A	0x40012000 to 0x4001EFFF
CMSDK AHB GPIO #1	Yes	0x40011000 to 0x40011FFF
CMSDK AHB GPIO #0	Yes	0x40010000 to 0x40010FFF
CMSDK APB subsystem	Yes	0x40000000 to 0x4000FFFF
Reserved	N/A	0x20800000 to 0x20FFFFFF
ZBTSRAM 2 & 3 (2x32-bit). Reserved 8 MB, 4 MB available. The two SRAM blocks are interleaved.	Yes	0x20000000 to 0x207FFFFF
Reserved	N/A	0x01010000 to 0x1FFFFFFF
Reserved	N/A	0x00800000 to 0x00FFFFFF
ZBTSRAM 1 (64-bit). Wrapped. Only 4 MB ZBTSRAM fitted.	Yes	0x00400000 to 0x007FFFFF
ZBTSRAM 1 (64-bit)	Yes	0x00004000 to 0x003FFFFF
Mappable memory. When <code>zbt_boot_ctrl</code> = 0, ZBTSRAM 1 is mapped to this region. Otherwise, <code>Remap_ctrl</code> = 0 maps Block RAM and <code>Remap_ctrl</code> = 1 maps ZBTSRAM 1. The V2M-MPS2 board microcontroller controls the <code>zbt_boot_ctrl</code> signal. The <code>zbt_boot_ctrl</code> signal overrides the boot option to enable use of the ZBT RAM.	Yes	0x00000000 to 0x00003FFF

5.2 MPS2 memory map for models with the Armv8-M additions

This section describes the MPS2 memory map for newer cores, with the Armv8-M additions.

For standard Arm peripherals, see the TRM for that device.



- A bus error is generated for accesses to memory areas not shown in this table.
- Any memory device that does not occupy the total region is aliased within that region.

Table 5-2: Memory map for models with the Armv8-M additions

Description	IDAU	Modeled	Address range
ZBTSRAM 1 (4 MB) in Non-secure (NS) world. Reserved 8 MB, only 4 MB implemented. VTOR initialization value to be configurable in LAC . Second half (4 MB) aliased to first half (4 MB).	NS	Yes	0x00000000 to 0x007FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x00800000 to 0x0FFFFFFF
ZBTSRAM 1 (4 MB) in Secure (S) world. Reserved 8 MB, only 4 MB implemented. Second half (4 MB) aliased to first half (4 MB).	S	Yes	0x10000000 to 0x107FFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0x10800000 to 0x1FFFFFFF
ZBTSRAM 2 and ZBTSRAM 3 (4 MB) in NS world. Reserved 8 MB, only 4 MB implemented. For IoT subsystems, different cores have different memory sizes. Second half (4 MB) aliased to first half (4 MB).	NS	Yes	0x20000000 to 0x207FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x20800000 to 0x20FFFFFFF
PSRAM (32 MB)	NS	Yes	0x21000000 to 0x22FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x23000000 to 0x23FFFFFFF
MTB SRAM. Reserved 64 KB, only 16 KB implemented. Aliased to 0x0 for booting in RTL simulation.	NS	Yes	0x24000000 to 0x2400FFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x24010000 to 0x2FFFFFFF
ZBTSRAM 2 and ZBTSRAM 3 (4 MB) in S world. Reserved 8 MB, only 4 MB implemented. Second half (4 MB) aliased to first half (4 MB).	S	Yes	0x30000000 to 0x307FFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0x30800000 to 0x30FFFFFFF
Not used. No memory gating unit on PSRAM (16 MB) path because it is shared with Ethernet control. Default expansion port: bus error.	S	N/A	0x31000000 to 0x31FFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0x30800000 to 0x3FFFFFFF
Timer 0. Non-secure CMSDK APB subsystem.	NS	Yes	0x40000000 to 0x40000FFF
Timer 1. Non-secure CMSDK APB subsystem.	NS	Yes	0x40001000 to 0x40001FFF
Dual Timer. Non-secure CMSDK APB subsystem.	NS	Yes	0x40002000 to 0x40002FFF
Not used. Non-secure CMSDK APB subsystem.	NS	N/A	0x40003000 to 0x40003FFF

Description	IDAU	Modeled	Address range
UART #0. Non-secure CMSDK APB subsystem.	NS	Yes	0x40004000 to 0x40004FFF
UART #1. Non-secure CMSDK APB subsystem.	NS	Yes	0x40005000 to 0x40005FFF
UART #2. Non-secure CMSDK APB subsystem.	NS	Yes	0x40006000 to 0x40006FFF
Not used. Non-secure CMSDK APB subsystem.	NS	N/A	0x40007000 to 0x40007FFF
Watchdog. Non-secure CMSDK APB subsystem.	NS	Yes	0x40008000 to 0x40008FFF
Not used. Non-secure CMSDK APB subsystem.	NS	N/A	0x40009000 to 0x4000F000
GPIO #0.	NS	Yes	0x40010000 to 0x40010FFF
GPIO #1.	NS	Yes	0x40011000 to 0x40011FFF
GPIO #2.	NS	Yes	0x40012000 to 0x40012FFF
GPIO #3.	NS	Yes	0x40013000 to 0x40013FFF
Default slave inside AHB peripheral subsystem. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	Yes	0x40014000 to 0x40017FFF
DMA Controller #0.	NS	Yes	0x40018000 to 0x40018FFF
DMA Controller #1.	NS	Yes	0x40019000 to 0x40019FFF
Default slave inside AHB peripheral subsystem. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	Yes	0x4001A000 to 0x4001EFFF
CMSDK system controller. PMU control and remap registers unused. Only reset option (lockup reset) and rest info available.	NS	Yes	0x4001F000 to 0x4001FFFF
Not used. Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	N/A	0x40020000 to 0x40020FFF
PL022 (SPI for LCD). Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Partial	0x40021000 to 0x40021FFF
SBCon I2C (Touch for LCD). Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Partial	0x40022000 to 0x40022FFF
SBCon I2C (Audio configuration). Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Yes	0x40023000 to 0x40023FFF
Audio I2S. Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Partial	0x40024000 to 0x40024FFF
Not used. Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	N/A	0x40025000 to 0x40027FFF
FPGA system control & I/O (LEDs, buttons...). Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Yes	0x40028000 to 0x40028FFF
Not used. Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	N/A	0x40029000 to 0x4002EFFF

Description	IDAU	Modeled	Address range
SCC registers. Non-secure FPGA APB subsystem (unused APB space: RAZ/WI).	NS	Yes	0x4002F000 to 0x4002FFFF
Not used.	NS	N/A	0x40030000 to 0x40113FFF
SVOS DualTimer. Only enabled for Cortex-M55 SVOS.	NS	Yes	0x40114000 to 0x40114fff
Not used.	NS	N/A	0x40115000 to 0x401FFFFF
Ethernet (SMSC 91C111).	NS	Partial	0x40200000 to 0x402FFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x40300000 to 0x40FFFFFF
VGA console.	NS	Yes	0x41000000 to 0x4100FFFF
Not used.	NS	N/A	0x41010000 to 0x410FFFFF
VGA image.	NS	Yes	0x41100000 to 0x4113FFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x41140000 to 0x4FFFFFFF
Timer 0. Secure CMSDK APB subsystem.	S	Yes	0x50000000 to 0x50000FFF
Timer 1. Secure CMSDK APB subsystem.	S	Yes	0x50001000 to 0x50001FFF
Dual Timer. Secure CMSDK APB subsystem.	S	Yes	0x50002000 to 0x50002FFF
Not used. Secure CMSDK APB subsystem.	S	N/A	0x50003000 to 0x50003FFF
UART #0. Secure CMSDK APB subsystem.	S	Yes	0x50004000 to 0x50004FFF
UART #1. Secure CMSDK APB subsystem.	S	Yes	0x50005000 to 0x50005FFF
UART #2. Secure CMSDK APB subsystem.	S	Yes	0x50006000 to 0x50006FFF
Not used. Secure CMSDK APB subsystem.	S	N/A	0x50007000 to 0x50007FFF
Watchdog. Secure CMSDK APB subsystem.	S	Yes	0x50008000 to 0x50008FFF
Not used. Secure CMSDK APB subsystem.	S	N/A	0x50009000 to 0x5000F000
GPIO #0	S	Yes	0x50010000 to 0x50010FFF
GPIO #1	S	Yes	0x50011000 to 0x50011FFF
GPIO #2	S	Yes	0x50012000 to 0x50012FFF

Description	IDAU	Modeled	Address range
GPIO #3	S	Yes	0x50013000 to 0x50013FFF
Default slave. Default expansion port: bus error.	S	Yes	0x50014000 to 0x50017FFF
DMA Controller #0.	S	Yes	0x50018000 to 0x50018FFF
DMA Controller #1.	S	Yes	0x50019000 to 0x50019FFF
Default slave. Default expansion port: bus error.	S	Yes	0x5001A000 to 0x5001EFFF
CMSDK system controller. PMU control and remap registers unused. Only reset option (lockup reset) and rest info available.	S	Yes	0x5001F000 to 0x5001FFFF
FPGA APB subsystem	S	-	0x50020000 to 0x5002FFFF
Not used. Secure FPGA APB subsystem	S	N/A	0x50020000 to 0x50020FFF
PL022 (SPI for LCD). Secure FPGA APB subsystem	S	Partial	0x50021000 to 0x50021FFF
SBCon I2C (touch for LCD). Secure FPGA APB subsystem	S	Partial	0x50022000 to 0x50022FFF
SBCon I2C (audio configuration). Secure FPGA APB subsystem	S	Yes	0x50023000 to 0x50023FFF
Audio I2S. Secure FPGA APB subsystem	S	Partial	0x50024000 to 0x50024FFF
Not used. Secure FPGA APB subsystem	S	N/A	0x50025000 to 0x50027FFF
FPGA system control & I/O (LEDs, buttons...). Secure FPGA APB subsystem	S	Yes	0x50028000 to 0x50028FFF
Not used. Secure FPGA APB subsystem	S	N/A	0x50029000 to 0x5002EFFF
SCC registers. Secure FPGA APB subsystem	S	Yes	0x5002F000 to 0x5002FFFF
Not used.	S	N/A	0x50030000 to 0x50113FFF
SVOS DualTimer. Only enabled for Cortex-M55 SVOS.	S	Yes	0x50114000 to 0x50114fff
Not used.	S	N/A	0x50115000 to 0x501FFFFF
Ethernet (SMSC 91C111).	S	Partial	0x50200000 to 0x502FFFFF
Not used. Default expansion port: bus error.	S	N/A	0x50300000 to 0x50FFFFFF
VGA console.	S	Yes	0x51000000 to 0x5100FFFF
Not used.	S	N/A	0x51010000 to 0x510FFFFFFF

Description	IDAU	Modeled	Address range
VGA image.	S	Yes	0x51100000 to 0x5113FFFF
Not used.	S	N/A	0x51140000 to 0x58006FFF
Secure Control Registers. Secure APB subsystem.	S	Yes	0x58007000 to 0x58007FFF
Flash memory gating unit configuration (mapped to AHB port for CODE region in the bus matrix, not APB). Secure APB subsystem.	S	Yes	0x58008000 to 0x58009FFF
SRAM memory gating unit configuration (mapped to AHB port for SRAM region in the bus matrix, not APB). Secure APB subsystem.	S	Yes	0x5800A000 to 0x5800DFFF
Reserved. Secure APB subsystem.	S	N/A	0x5800E000 to 0x5800EFFF
Reserved. Secure APB subsystem.	S	N/A	0x5800F000 to 0x5800FFFF
Not used. Default expansion port: bus error.	S	N/A	0x58010000 to 0x5FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x60000000 to 0x6FFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0x70000000 to 0x7FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0x80000000 to 0x8FFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0x90000000 to 0x9FFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0xA0000000 to 0xAFFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0xB0000000 to 0xBFFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0xC0000000 to 0xCFFFFFFF
Not used. Default expansion port: bus error.	S	N/A	0xD0000000 to 0xDFFFFFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0xE0000000 to 0xEFFFFFFF
System ROM table. Exempted from checking.	Exempt	Yes	0xF0000000 to 0xF0000FFF
Not used. Default expansion port: bus error.	Exempt	N/A	0xF0001000 to 0xF000FFFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0xF0100000 to 0xF01FFFFF
MTB SFR address space.	NS	Yes	0xF0200000 to 0xF0200FFF
Reserved. This region is non-executable.	NS	N/A	0xF0210000 to 0xF0213FFF
Not used. Default expansion port (MPS2 AHB subsystem): bus error or RAZ/WI .	NS	N/A	0xF0214000 to 0xFFFFFFFF

5.3 MPS2 interrupt assignments

This section describes the interrupt assignments.

Table 5-3: Interrupt assignments

Number	Interrupt
NMI	Watchdog.
0	UART 0 receive interrupt.
1	UART 0 transmit interrupt.
2	UART 1 receive interrupt.
3	UART 1 transmit interrupt.
4	UART 2 receive interrupt.
5	UART 2 transmit interrupt.
6	GPIO 0, 2 combined interrupt.
7	GPIO 1, 3 combined interrupt.
8	Timer 0.
9	Timer 1.
10	Dual Timer.
11	SPI #1 (LCD). The LCD had shared SPI #0 and SPI #1.
12	UART overflow (0, 1, 2).
13	Ethernet.
14	Audio I2S.
15	Touch screen.
16-31	GPIO 0 individual interrupts.
32-47	GPIO 1 individual interrupts. Armv8-M additions.
48	SPI #0. Armv8-M addition.
49	Reserved.
50	TRNG (Secure). Armv8-M addition.
51	Unique ID and Secure storage (Secure). Armv8-M addition.
52	DMA controller #0.
53	DMA controller #1.
54	SecureErrorIRQ. Armv8-M addition. Detection of Non-secure access to Secure address spaces, including other bus masters. Generated by Memory Gating unit, Peripheral Gating units, and bus gasket for legacy bus masters.

5.4 Differences between MPS2 FVPs and hardware implementations

This section describes the features of the hardware that the models do not implement, or implement with significant differences.

MPS2 implements most devices. Some peripherals have minimal implementations:

- The Ethernet module in the model is a LAN91C111. The hardware provides a LAN9220.
- The Audio module is **RAZ/WI**.
- The STMPE811 touchscreen module only reports touch positions.
- The model of the Ampire LCD module supports a subset of the graphics modes.

You can display images and text on an emulated VGA output, images on the LCD, and text on the UART.

RX overrun mode

The CMSDK_UART component has a parameter `rx_overrun_mode` that controls how to handle the transfer of characters into the UART RX FIFO when the `RX_OVERRUN` flag is set in the STATE register. It has the following possible values:

0

This is the default value. Never block the transfer of the next character into the RX FIFO even if it means losing multiple characters. This is the same behavior as the hardware. It might be useful when evaluating software design, for example to indicate whether the UART can be serviced quickly enough.

In this mode, as in the hardware, the `RX_OVERRUN` flag serves only to alert software to the fact that characters have been lost and that some sort of corrective action, or recovery procedure might be required.

1

Pause the transfer of characters into the RX FIFO before any characters are lost. This makes the serial connection lossless even if the software does not make any attempt to service the UART in a timely fashion.

In this mode, the transfer of characters can be resumed by reading a character from the DATA register, so no special action is required by software.

2

Pause the transfer of characters into the UART RX FIFO after the first character is lost due to overrun.

In this mode, clearing the `RX_OVERRUN` flag resumes the transfer of characters. This requires the software to write to the STATE or INT register to clear the flag. Precisely one character will have been lost. This is the legacy behavior of the UART.

Arm®v8-M

The model does not support MTB, ETM, and TPIU. MTB RAM is absent.

In the Memory Gating Unit, the model provides a configurable block size. For performance reasons, the minimum block size in the model is 4096 bytes. Hardware and later models might allow smaller block sizes. Software must use the BLK_CFG register to determine block size.

Timing

FVPs enable software applications to run in a functionally accurate simulation. However, because of the relative balance of fast simulation speed over timing accuracy, there are situations where the models might behave unexpectedly.

If your code interacts with real world devices such as timers and keyboards, data arrives in the modeled device in real world, or wall clock, time. However, simulation time can run faster than the wall clock. So, a single key press might be interpreted as several repeated key presses, or a single mouse click might be interpreted as a double click.

To avoid this mismatch, the FVPs provide the Rate Limit feature. Enabling Rate Limit forces the model to run at wall clock time. For interactive applications, Arm recommends enabling Rate Limit. Use the Rate Limit button in the CLCD display or the `rate_limit-enable` model instantiation parameter.

5.5 MPS2 platform types

Configure the MPS2 FVP platform type using the `fvp_mps2.platform_type` parameter.

It has the following possible values:

0

This value is the default. The FVP acts as a V2M-MPS2 system, with the additions for v8-M, as specified in the Arm®v8-M MPS2 System Specification (ECM 0468897), v0.8. This specification is confidential and is available only to licensed Arm customers. For details, contact your Arm support representative.

1

The FVP acts as an IoT Kit on an MPS2+ board. For details, see the following documents:

- [Cortex®-M23 processor Arm®v8-M IoT Kit User Guide \(ECM 0635473\)](#).
- [Cortex®-M33 processor Arm®v8-M IoT Kit User Guide \(ECM 0601256\)](#).

2

The FVP acts as an Arm® CoreLink™ SSE-200 Subsystem on an MPS2+ board. For details, see [AN521 - Example SSE-200 Subsystem for MPS2+ Application Note](#).

5.6 MPS2 Platform FVPs

This section lists the instances in each FVP.

5.6.1 Instances for FVP_MPS2_AEMv8M

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_AEMv8M](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_AEMv8M
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIidentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl

- [IoTSS_SystemInfo](#)
- [LabellerIdauSecurity](#)
- [MPS2_Audio](#)
- [MPS2_LCD](#)
- [MPS2_SecureCtrl](#)
- [MPS2_TouchScreen](#)
- [MPS2_VGA](#)
- [MPS2_Visualisation](#)
- [OrGate](#)
- [PDCM](#)
- [PL022_SSP_MPS2](#)
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SSE200](#)
- [SVOS_DualTimer](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [SecurityModifier](#)
- [SignalRouter](#)
- [TelnetTerminal](#)
- [VIOBridge](#)
- [VSIBridge](#)
- [VSocketBridge](#)
- [WarningMemory](#)

5.6.2 Instances for FVP_MPS2_Cortex-M0

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M0](#)

- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M0
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo
- [LabellerIdauSecurity](#)
- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)

- PDCM
- PL022_SSP_MPS2
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- SSE200
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.3 Instances for FVP_MPS2_Cortex-M0plus

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M0+](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)

- [CounterModule](#)
- [DebugAccessPort](#)
- [FPGA_SysCtrl](#)
- [FVP_MPS2](#)
- [FVP_MPS2_Cortex_M0plus](#)
- [GPIO1_Connection_Test](#)
- [GPIO_Connection_Test](#)
- [GPIO_Port_Transfer](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IoTSS_AccessControlGate](#)
- [IoTSS_CPUIidentity](#)
- [IoTSS_MemoryProtectionController](#)
- [IoTSS_MessageHandlingUnit](#)
- [IoTSS_PeripheralProtectionController](#)
- [IoTSS_SystemControl](#)
- [IoTSS_SystemInfo](#)
- [LabellerIdauSecurity](#)
- [MPS2_Audio](#)
- [MPS2_LCD](#)
- [MPS2_SecureCtrl](#)
- [MPS2_TouchScreen](#)
- [MPS2_VGA](#)
- [MPS2_Visualisation](#)
- [OrGate](#)
- [PDCM](#)
- [PL022_SSP_MPS2](#)
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)

- SSE200
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.4 Instances for FVP_MPS2_Cortex-M3

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M3](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M3
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)

- [HostBridge](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo
- [LabellerIdauSecurity](#)
- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)
- PDCM
- PL022_SSP_MPS2
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- SSE200
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge

- [VSocketBridge](#)
- [WarningMemory](#)

5.6.5 Instances for FVP_MPS2_Cortex-M4

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M4](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M4
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo
- [LabellerIdauSecurity](#)

- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)
- PDCM
- PL022_SSP_MPS2
- [PL080_DMAC](#)
- PPUv0
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- SSE200
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.6 Instances for FVP_MPS2_Cortex-M7

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M7](#)
- CMSDK_DualTimer
- CMSDK_GPIO

- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M7
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo
- [LabellerIdauSecurity](#)
- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)
- PDCM
- PL022_SSP_MPS2

- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SSE200](#)
- [SVOS_DualTimer](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [SecurityModifier](#)
- [SignalRouter](#)
- [TelnetTerminal](#)
- [VIOBridge](#)
- [VSIBridge](#)
- [VSocketBridge](#)
- [WarningMemory](#)

5.6.7 Instances for FVP_MPS2_Cortex-M23

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M23](#)
- [CMSDK_DualTimer](#)
- [CMSDK_GPIO](#)
- [CMSDK_SysCtrl](#)
- [CMSDK_Timer](#)
- [CMSDK_UART](#)
- [CMSDK_Watchdog](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)

- [FPGA_SysCtrl](#)
- [FVP_MPS2](#)
- [FVP_MPS2_Cortex_M23](#)
- [GPIO1_Connection_Test](#)
- [GPIO_Connection_Test](#)
- [GPIO_Port_Transfer](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- [IoTSS_CPUIIdentity](#)
- [IoTSS_MemoryProtectionController](#)
- [IoTSS_MessageHandlingUnit](#)
- [IoTSS_PeripheralProtectionController](#)
- [IoTSS_SystemControl](#)
- [IoTSS_SystemInfo](#)
- [LabellerIdauSecurity](#)
- [MPS2_Audio](#)
- [MPS2_LCD](#)
- [MPS2_SecureCtrl](#)
- [MPS2_TouchScreen](#)
- [MPS2_VGA](#)
- [MPS2_Visualisation](#)
- [OrGate](#)
- [PDCM](#)
- [PL022_SSP_MPS2](#)
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SSE200](#)

- [STLBusGasket](#)
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.8 Instances for FVP_MPS2_Cortex-M33

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M33](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- [DebugAccessPort](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M33
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)

- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- [IoTSS_CPUIidentity](#)
- [IoTSS_MemoryProtectionController](#)
- [IoTSS_MessageHandlingUnit](#)
- [IoTSS_PeripheralProtectionController](#)
- [IoTSS_SystemControl](#)
- [IoTSS_SystemInfo](#)
- [LabellerIdauSecurity](#)
- [MPS2_Audio](#)
- [MPS2_LCD](#)
- [MPS2_SecureCtrl](#)
- [MPS2_TouchScreen](#)
- [MPS2_VGA](#)
- [MPS2_Visualisation](#)
- [OrGate](#)
- [PDCM](#)
- [PL022_SSP_MPS2](#)
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SSE200](#)
- [SVOS_DualTimer](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [SecurityModifier](#)
- [SignalRouter](#)
- [TelnetTerminal](#)
- [VIOBridge](#)

- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.9 Instances for FVP_MPS2_Cortex-M52

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M52](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M52
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo

- [LabellerIdauSecurity](#)
- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)
- PDCM
- PL022_SSP_MPS2
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- SSE200
- [STLBusGasket](#)
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.10 Instances for FVP_MPS2_Cortex-M55

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M55](#)

- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [CounterModule](#)
- FPGA_SysCtrl
- FVP_MPS2
- FVP_MPS2_Cortex_M55
- GPIO1_Connection_Test
- GPIO_Connection_Test
- GPIO_Port_Transfer
- [GUIPoll](#)
- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- IoTSS_CPUIdentity
- IoTSS_MemoryProtectionController
- IoTSS_MessageHandlingUnit
- [IoTSS_PeripheralProtectionController](#)
- IoTSS_SystemControl
- IoTSS_SystemInfo
- [LabellerIdauSecurity](#)
- MPS2_Audio
- MPS2_LCD
- MPS2_SecureCtrl
- MPS2_TouchScreen
- MPS2_VGA
- MPS2_Visualisation
- [OrGate](#)

- PDCM
- PL022_SSP_MPS2
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- SSE200
- [STLBusGasket](#)
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

5.6.11 Instances for FVP_MPS2_Cortex-M85

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-M85](#)
- CMSDK_DualTimer
- CMSDK_GPIO
- CMSDK_SysCtrl
- [CMSDK_Timer](#)
- CMSDK_UART
- CMSDK_Watchdog
- [ClockDivider](#)
- [ClockTimerThread](#)

- [ClockTimerThread64](#)
- [CounterModule](#)
- [FPGA_SysCtrl](#)
- [FVP_MPS2](#)
- [FVP_MPS2_Cortex_M85](#)
- [GPIO1_Connection_Test](#)
- [GPIO_Connection_Test](#)
- [GPIO_Port_Transfer](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IDAU](#)
- [IoTSS_AccessControlGate](#)
- [IoTSS_CPUIdentity](#)
- [IoTSS_MemoryProtectionController](#)
- [IoTSS_MessageHandlingUnit](#)
- [IoTSS_PeripheralProtectionController](#)
- [IoTSS_SystemControl](#)
- [IoTSS_SystemInfo](#)
- [LabellerIdauSecurity](#)
- [MPS2_Audio](#)
- [MPS2_LCD](#)
- [MPS2_SecureCtrl](#)
- [MPS2_TouchScreen](#)
- [MPS2_VGA](#)
- [MPS2_Visualisation](#)
- [OrGate](#)
- [PDCM](#)
- [PL022_SSP_MPS2](#)
- [PL080_DMAC](#)
- [PPUv0](#)
- [PVBusExclusiveMonitor](#)
- [PVBusExclusiveSquasher](#)
- [PVBusRouter](#)
- [RAMDevice](#)

- [SMSC_91C111](#)
- SSE200
- [STLBusGasket](#)
- SVOS_DualTimer
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- SecurityModifier
- SignalRouter
- [TelnetTerminal](#)
- VIOBridge
- VSIBridge
- VSocketBridge
- [WarningMemory](#)

6. Versatile Express

This chapter describes the components of Fast Models that are specific to the Versatile™ Express (VE) model of the hardware platform.



The VE platform FVPs are deprecated and will be removed in a future release.

6.1 VE

The Versatile Express (VE) FVPs are functionally-accurate system models for software execution.



The VE FVPs are deprecated and will be removed in a future release.

Arm produces the VE hardware development platform. The Motherboard Express μAdvanced Technology Extended (ATX) V2M-P1 is the basis for an integrated software and hardware development system. This system is also based on the Arm Symmetric MultiProcessor (SMP) system architecture.

The VE FVPs are system models implemented in software. Each model contains:

- A virtual implementation of the Arm VE motherboard.
- A single daughterboard containing one or more Arm processors.
- Associated interconnections.

The motherboard provides:

- Peripherals for multimedia or networking environments.
- Access to motherboard peripherals and functions through a static memory bus to simplify access from daughterboards.
- High-performance PCI-Express slots for expansion cards.
- Consistent memory maps with different processor daughterboards that simplify software development and porting.
- Automatic detection and configuration of attached CoreTile Express and LogicTile Express daughterboards.
- Automatic shutdown for over-temperature or power supply failure.
- No system power-on for unconfigurable daughterboards.

- Power sequencing of system.
- Drag and drop file updating of configuration files.
- Support of either a 12V power-supply unit or an external ATX power supply.
- Support of FPGA and processor daughterboards to provide custom peripherals, early access to processor designs, or production test chips.



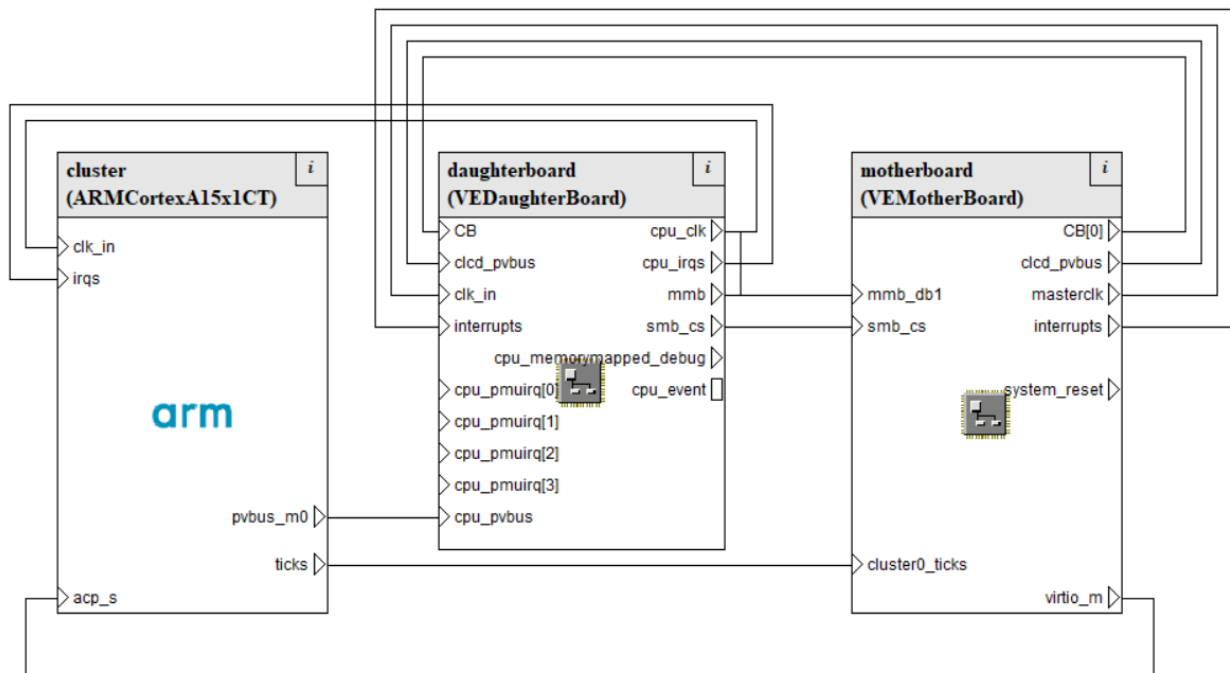
Note

Arm bases the models on the VE platform memory map, but does not intend them to be accurate representations of a specific VE hardware revision. The VE FVPs support selected peripherals. The models are sufficiently complete and accurate to boot the same operating system images as the VE hardware.

VE FVPs provide functionally-accurate models for software execution. However, the models sacrifice timing accuracy to increase simulation speed. Key deviations from hardware are:

- Approximate timing.
- Simplified buses.
- No implementations for processor caches and the related write buffers.

Figure 6-1: Top-level block diagram of a VE model



Related information

[ARM Motherboard Express µATX V2M-P1 Technical Reference Manual](#)

6.2 VE memory map for Cortex-A series

The global memory map for the Cortex®-A series VE model is based on the hardware Versatile™ Express RS1 memory map with the RS2 extensions.



Note

The VE FVP implementation of memory does not require the memory controller to have the correct values. If you run applications on hardware, ensure that the memory controller is set up properly. Otherwise, applications that run on the FVP might fail on hardware.

Table 6-1: Cortex®-A series platform model memory map

Name	Modeled	Address range	Size
NOR FLASH0 (CS0)	Yes	0x00_00000000-0x00_03FFFFFF	64 MB
Reserved	-	0x00_04000000-0x00_07FFFFFF	64 MB
NOR FLASH0 alias (CS0)	Yes	0x00_08000000-0x00_0BFFFFFF	64 MB
NOR FLASH1 (CS4)	Yes	0x00_0C000000-0x00_0FFFFFFF	64 MB
Unused (CS5)	-	0x00_10000000-0x00_13FFFFFF	-
PSRAM (CS1) - unused	No	0x00_14000000-0x00_17FFFFFF	-
Peripherals (CS2). See Table: CS2 region peripheral memory map, below.	Yes	0x00_18000000-0x00_1BFFFFFF	64 MB
Peripherals (CS3). See Table: CS2 region peripheral memory map, below.	Yes	0x00_1C000000-0x00_1FFFFFFF	64 MB
CoreSight™ and peripherals	No	0x00_20000000-0x00_2CFFFFFF. See Note after table.	-
Graphics space	No	0x00_2D000000-0x00_2D00FFFF	-
System SRAM	Yes	0x00_2E000000-0x00_2EFFFFFF	64 KB
Ext AXI	No	0x00_2F000000-0x00_7FFFFFFF	-
4 GB DRAM (in 32-bit address space). See Note after table.	Yes	0x00_80000000-0x00_FFFFFFFF	2 GB
Unused	-	0x01_00000000-0x07_FFFFFFFF	-
4 GB DRAM (in 36-bit address space). See Note after table.	Yes	0x08_00000000-0x08_FFFFFFFF	4 GB
Unused	-	0x09_00000000-0x7F_FFFFFFFF	-
4 GB DRAM (in 40-bit address space). See Note after table.	Yes	0x80_00000000-0xFF_FFFFFFFF	4 GB



Note

- The private peripheral address 0x2c000000 is mapped in the CoreSight™ and peripherals region. Use the parameter `PERIPHBASE` to map the peripherals to a different address.
- The model contains a single 4 GB block of DRAM, which is aliased across the three different DRAM regions.

In other words, it can be accessed at three different physical addresses, which are all mapped to the same area of DRAM.

For example, a write to address `0x00_80000000` is visible to reads at address `0x80_00000000`.

The lowest of the physical address regions is only 2 GB in size.

The model has a `secure_memory` option. When you enable this option, the memory map changes for a number of peripherals.

Table 6-2: CS2 region peripheral memory map for `secure_memory` option

Peripheral	Address range	Functionality with <code>secure_memory</code> enabled
NOR FLASH0 (CS0)	<code>0x00_00000000-0x00_0001FFFF</code>	Secure RO, aborts on non-secure accesses.
Reserved	<code>0x00_04000000-0x00_0401FFFF</code>	Secure SRAM, aborts on non-secure accesses.
NOR FLASH0 alias (CS0)	<code>0x00_08000000-0x00_7DFFFFFF</code>	Normal memory map, aborts on secure accesses.
Ext AXI	<code>0x00_7e000000-0x00_7FFFFFFF</code>	Secure DRAM, aborts on non-secure accesses.
4 GB DRAM in 32-bit address space	<code>0x00_80000000-0xFF_FFFFFFFF</code>	Normal memory map, aborts on secure accesses.

Table 6-3: CS2 region peripheral memory map

Peripheral	Modeled	Address range	Size	GIC Int. See Note after table.
VRAM - aliased	Yes	<code>0x00_18000000-0x00_19FFFFFF</code>	32MB	-
Ethernet (SMSC 91C111)	Yes	<code>0x00_1A000000-0x00_1AFFFFFF</code>	16MB	47
USB - unused	No	<code>0x00_1B000000-0x00_1BFFFFFF</code>	16MB	-



Use these interrupt signal values to program your interrupt controller. They are the SPI number plus 32.

Add 32 to the interrupt number from the peripherals to form the interrupt number that the GIC sees. GIC interrupts 0-31 are for internal use.

Table 6-4: CS3 region peripheral memory map

Peripheral	Modeled	Address range	Size	GIC Int. See Note after table.
Local DAP ROM	No	<code>0x00_1C000000-0x00_1C00FFFF</code>	64 KB	-
VE System Registers	Yes	<code>0x00_1C010000-0x00_1C01FFFF</code>	64 KB	-
System Controller (SP810)	Yes	<code>0x00_1C020000-0x00_1C02FFFF</code>	64 KB	-
TwoWire serial interface (PCIe)	No	<code>0x00_1C030000-0x00_1C03FFFF</code>	64 KB	-
AACI (PL041)	Yes	<code>0x00_1C040000-0x00_1C04FFFF</code>	64 KB	43
MCI (PL180)	Yes	<code>0x00_1C050000-0x00_1C05FFFF</code>	64 KB	41, 42
KMI - keyboard (PL050)	Yes	<code>0x00_1C060000-0x00_1C06FFFF</code>	64 KB	44
KMI - mouse (PL050)	Yes	<code>0x00_1C070000-0x00_1C07FFFF</code>	64 KB	45
Reserved	-	<code>0x00_1C080000-0x00_1C08FFFF</code>	64 KB	-

Peripheral	Modeled	Address range	Size	GIC Int. See Note after table.
UART0 (PL011)	Yes	0x00_1C090000-0x00_1C09FFFF	64 KB	37
UART1 (PL011)	Yes	0x00_1C0A0000-0x00_1C0AFFFF	64 KB	38
UART2 (PL011)	Yes	0x00_1C0B0000-0x00_1C0BFFFF	64 KB	39
UART3 (PL011)	Yes	0x00_1C0C0000-0x00_1C0CFFFF	64 KB	40
Reserved	-	0x00_1C0D0000-0x00_1C0EFFFF	128 KB	-
Watchdog (SP805)	Yes	0x00_1C0F0000-0x00_1C0FFFFF	64 KB	32
Reserved	-	0x00_1C100000-0x00_1C10FFFF	64 KB	-
Timer-0 (SP804)	Yes	0x00_1C110000-0x00_1C11FFFF	64 KB	34
Timer-1 (SP804)	Yes	0x00_1C120000-0x00_1C12FFFF	64 KB	35
Virtio block device	Yes	0x00_1C130000-0x00_1C13FFFF	64 KB	74
Virtio P9 device	Yes	0x00_1C140000-0x00_1C14FFFF	64 KB	75
Reserved	-	0x00_1C130000-0x00_1C15FFFF	192 KB	-
TwoWire serial interface (DVI) - unused	No	0x00_1C160000-0x00_1C16FFFF	64 KB	-
Real-time Clock (PL031)	Yes	0x00_1C170000-0x00_1C17FFFF	64 KB	36
Reserved	-	0x00_1C180000-0x00_1C19FFFF	128 KB	-
CF Card - unused	No	0x00_1C1A0000-0x00_1C1AFFFF	64 KB	
Reserved	-	0x00_1C1B0000-0x00_1C1EFFFF	256 KB	-
Color LCD Controller (PL111)	Yes	0x00_1C1F0000-0x00_1C1FFFFF	64 KB	46
Reserved	-	0x00_1C200000-0x00_1FFFFFFF	64 KB	-

**Note**

Use these interrupt signal values to program your interrupt controller. They are the SPI number plus 32.

Add 32 to the interrupt number from the peripherals to form the interrupt number that the GIC sees. GIC interrupts 0-31 are for internal use.

6.3 VE memory map for Cortex-R series

The Versatile™ Express RS1 memory map with the RS2 extensions is the base of the global memory map for the Cortex®-R series platform model.

Table 6-5: Cortex®-R series VE FVP memory map

Memory	Modeled	Address range
DRAM	Yes	0x00000000-0x3FFFFFFF
FLASH0	Yes	0x40000000-0x43FFFFFF
FLASH1	Yes	0x44000000-0x47FFFFFF
PSRAM	Yes	0x48000000-0x4BFFFFFF
RAM	No	0x4C000000-0x4FFFFFFF
PL390 GIC CPU Interface. Cortex®-R4 and Cortex®-R5 models only.	Yes	0xAE000000-0xAE00FFFF

Memory	Modeled	Address range
PL390 GIC Distributor. Cortex®-R4 and Cortex®-R5 models only.	Yes	0xAE001000-0xAE001FFF
VE System Registers	Yes	0xB0000000-0xB000FFFF
SP810	Yes	0xB0010000-0xB001FFFF
PL041 AACI	Yes	0xB0040000-0xB004FFFF
PL180 MCI	Yes	0xB0050000-0xB005FFFF
PL050 KMI0	Yes	0xB0060000-0xB006FFFF
PL050 KMI1	Yes	0xB0070000-0xB007FFFF
PL011 UART0	Yes	0xB0090000-0xB009FFFF
PL011 UART1	Yes	0xB00A0000-0xB00AFFFF
PL011 UART2	Yes	0xB00B0000-0xB00BFFFF
PL011 UART3	Yes	0xB00C0000-0xB00CFFFF
SP805 WATCHDOG	Yes	0xB00F0000-0xB00FFFFF
TIMER_0_1	Yes	0xB0110000-0xB011FFFF
TIMER_2_3	Yes	0xB0120000-0xB012FFFF
PL031 Real Time Clock	Yes	0xB0170000-0xB017FFFF
Compact Flash	No	0xB01A0000-0xB01AFFFF
PL011 UART4	Yes	0xB01B0000-0xB01BFFFF
PL111 CLCD	Yes	0xB01F0000-0xB01FFFFF. See Note after table
RAM	No	0xB4000000-0xBBFFFFFF
Video RAM	Yes	0xBC000000-0xBDFFFFFF
Ethernet (SMSC 91C111)	Yes	0xBE000000-0xBEFFFFFF
USB	No	0xBF000000-0xBFFFFFFF



For Cortex®-R4 and Cortex®-R5 models, the range for PL111 CLCD is
0xA0000000-0xA0010000

6.4 VE interrupt assignments for Cortex-A series

The platform routes the following Shared Peripheral Interrupts (SPIs) to the GIC.

Table 6-6: SPI GIC assignments

IRQ ID	SPI offset	Device
32	0	Watchdog, SP805
34	2	Dual timer 0/1, SP804
35	3	Dual timer 2/3, SP804
36	4	Real-time Clock, PL031
37	5	UART0, PL011
38	6	UART1, PL011

IRQ ID	SPI offset	Device
39	7	UART2, PL011
40	8	UART3, PL011
41	9	MCI, PL180, MCIINTR0
42	10	MCI, PL180, MCIINTR1
43	11	AACI, PL041
44	12	KMI - Keyboard, PL050
45	13	KMI - Mouse, PL050
46	14	Color LCD Controller, PL111
47	15	Ethernet, SMSC 91C111
74	42	Virtio block device
75	43	Virtio P9 device
92	60	CPU 0 PMU
93	61	CPU 1 PMU
94	62	CPU 2 PMU
95	63	CPU 3 PMU
117	85	HDLCD

6.5 VE interrupt assignments for Cortex-R series

These tables describe the interrupt assignments for Cortex-R4, Cortex-R5, Cortex-R7 and Cortex-R8.

Table 6-7: Interrupt assignments for Cortex-R4 and Cortex-R5

GIC IRQ ID	SPI offset	Device
32	0	Watchdog, SP805
34	2	Dual timer 0/1, SP804
35	3	Dual timer 2/3, SP804
36	4	Real-time Clock, PL031
41	9	MCI, PL180, MCIINTR0
42	10	MCI, PL180, MCIINTR1
43	11	AACI, PL041
44	12	KMI - Keyboard, PL050
45	13	KMI - Mouse, PL050
47	15	Ethernet, SMSC 91C111
75	16	Level 2 Cache Controller, PL310 Combined interrupt
76	14	Color LCD Controller, PL111
96	5	UART0, PL011
97	6	UART1, PL011
98	7	UART2, PL011
99	8	UART3, PL011

Table 6-8: Interrupt assignments for Cortex-R7 and Cortex-R8

GIC IRQ ID	SPI offset	Device
32	0	Watchdog, SP805
34	2	Dual timer 0/1, SP804
35	3	Dual timer 2/3, SP804
36	4	Real-time Clock, PL031
37	5	UART0, PL011
38	6	UART1, PL011
39	7	UART2, PL011
40	8	UART3, PL011
41	9	MCI, PL180, MCIINTR0
42	10	MCI, PL180, MCIINTR1
43	11	AACI, PL041
44	12	KMI - Keyboard, PL050
45	13	KMI - Mouse, PL050
46	14	Color LCD Controller, PL111
47	15	Ethernet, SMSC 91C111

6.6 VE parameters

This section describes the VE FVP instantiation parameters.

6.6.1 VE instantiation parameters

This table describes the instantiation parameters for VE models.

Table 6-9: VE instantiation parameters

Component	Parameter	Type	Allowed values	Default value	Description
ve_sysregs	user_switches_value	Integer	See VE switch S6 .	0	Switch S6 setting.
flashloader0	fname	String	Valid filename	""	Path to flash image file.
flashloader1	fname	String	Valid filename	""	Path to flash image file.
mmc	p_mmc_file	String	Valid filename	mmc.dat	Multimedia card filename.
pl111_clcd	pixel_double_limit	Integer	-	12c	Sets threshold in horizontal pixels below which pixels sent to framebuffer are doubled in size in both dimensions.
sp810_sysctrl	use_s8	Boolean	true, false	false	Indicates whether to read boot_switches_value.

6.6.2 VE secure memory parameters

This table describes the VE FVP secure memory parameters that you can change when you start the model.

Table 6-10: VE secure memory parameters

Name	Type	Allowed values	Default value	Description
daughterboard.secure_memory	Boolean	true, false	false	false The platform behaves as before. true The address space is segregated according to the security mode of the core. Some memory blocks near the bottom of the address space are available to Secure transactions only. The rest of the address space is available to Non-secure transactions only.

6.6.3 VE switch S6

This section describes the behavior and default positions of the VE system model switch.

Switch S6 is equivalent to the Boot Monitor configuration switch on the VE hardware.

If you have the standard Arm® Boot Monitor flash image loaded, the setting of switch S6-1 changes what happens on model reset. Otherwise, the function of switch S6 is implementation dependent.

To write the switch position directly to the S6 parameter in the model, you must convert the switch settings to an integer value from the equivalent binary, where 1 is on and 0 is off.

Table 6-11: Default positions of VE system model switch

Switch	Default position	Function in default position
S6-1	OFF	Displays prompt permitting Boot Monitor command entry after system start.
S6-2	OFF	See STDIO redirection, below.
S6-3	OFF	See STDIO redirection, below.
S6-4 to S6-8	OFF	Reserved for application use.

If S6-1 is in the ON position, the Boot Monitor executes the boot script that was loaded into flash. If there is no script, the Boot Monitor prompt is displayed.

The settings of S6-2 and S6-3 affect STDIO source and destination on model reset.

Table 6-12: STDIO redirection

S6-2	S6-3	Output	Input	Description
OFF	OFF	UART0	UART0	STDIO autodetects whether to use semihosting I/O or a UART. If a debugger is connected, STDIO is redirected to the debugger output window, otherwise STDIO goes to UART0.

S6-2	S6-3	Output	Input	Description
OFF	ON	UART0	UART0	STDIO is redirected to UART0, regardless of semihosting settings.
ON	OFF	CLCD	Keyboard	STDIO is redirected to the CLCD and keyboard, regardless of semihosting settings.
ON	ON	CLCD	UART0	STDIO output is redirected to the LCD and input is redirected to UART0, regardless of semihosting settings.

6.7 VE components

A complete model implementation of the VE platform includes both VE-specific components and generic components, such as buses and timers.

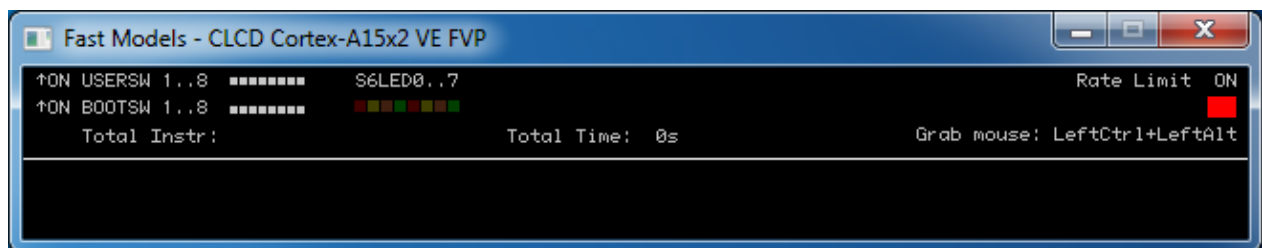
To see a list of all the component instances in the model, run it with the `--list-instances` option.

The generic components are documented in the [Fast Models Reference Guide](#).

6.7.1 VEVisualisation component

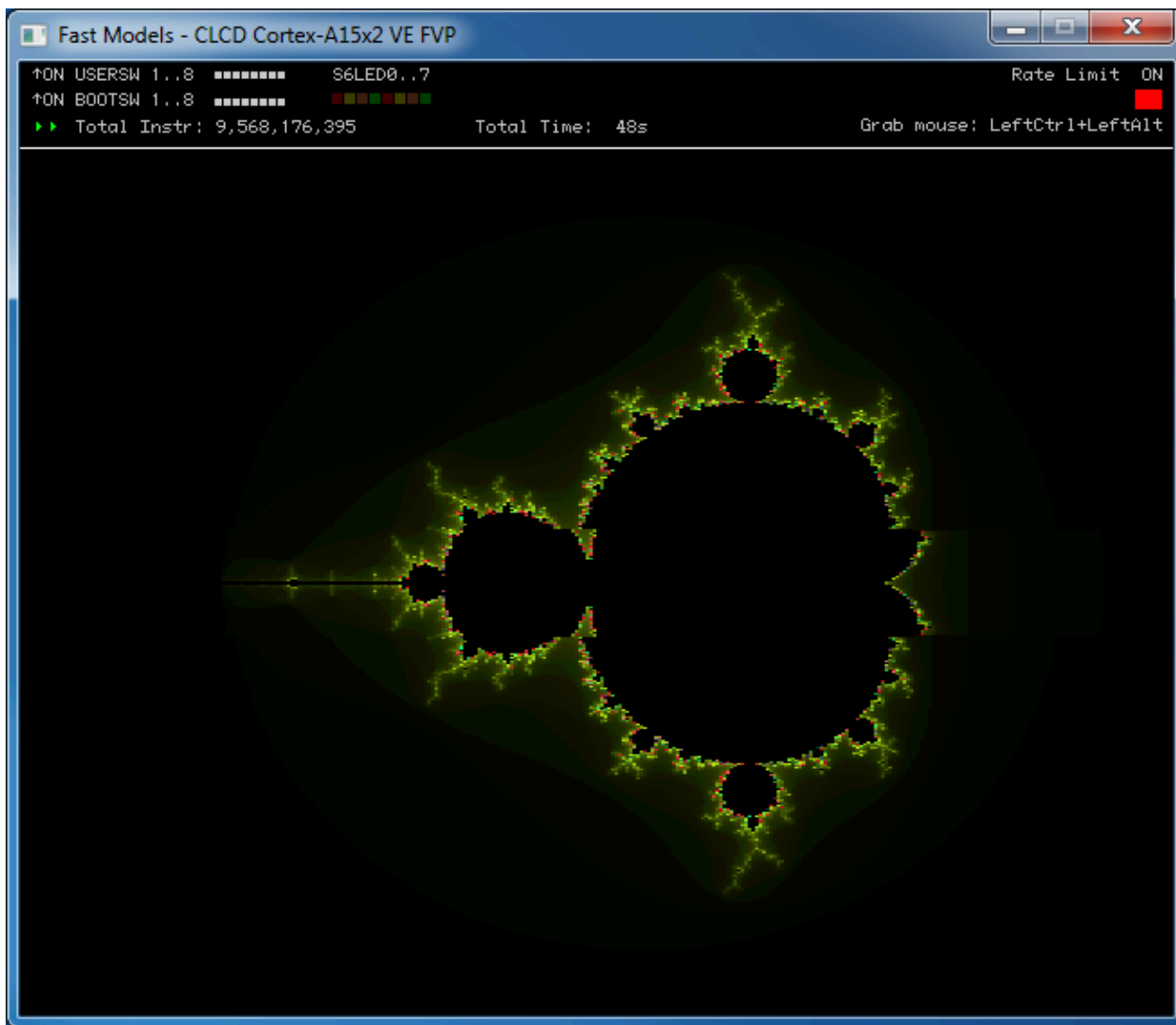
This component can generate events from the host mouse or keyboard when the visualization window is in focus. For example, you can toggle the switch elements from the visualization window.

Figure 6-2: VE FVP CLCD visualization window



When a suitable application or system image loads, and configures the PL111_CLCD controller registers, the window expands to show the contents of the framebuffer.

Figure 6-3: VE FVP CLCD with brot.axf image



Note

Using this component can reduce simulation performance. Use the `rate_limit-enable` parameter to control simulation speed.

6.7.1.1 VEEVisualisation ports

This section describes the VEEVisualisation component ports.

Table 6-13: VEEVisualisation ports

Name	Protocol	Type	Description
boot_switch	ValueState	Slave	Provides state for the eight Boot DIP switches on the right side of the CLCD status bar.
clock_50Hz	ClockSignal	Slave	50Hz clock input.
cluster0_ticks[4]	InstructionCount	Slave	Connection from processor model in cluster 0 to show its current instruction count.
cluster1_ticks[4]	InstructionCount	Slave	Connection from processor model in cluster 1 to show its current instruction count.
daughter_leds	ValueState	Slave	A read/write port to read and set the value of the LEDs. 1 bit per LED, LSB left-most, up to 32 LEDs available. The LEDs appear only when parameter <code>daughter_led_count</code> is set to nonzero.
daughter_user_switches	ValueState	Slave	A read port to return the value of the daughter user switches. Write to this port to set the value of the switches, and use during reset only. LSB is left-most, up to 32 switches available.
keyboard	KeyboardStatus	Master	Output port providing key change events when the visualization window is in focus.
lcd	LCD	Slave	Connection from a CLCD controller for visualization of the frame buffer.
lcd_layout	LCDLayoutInfo	Master	Layout information for alphanumeric LCD display.
leds	ValueState	Slave	Displays state using the eight colored LEDs on the status bar.
mouse	MouseStatus	Master	Output port providing mouse movement and button events when the visualization window is in focus.
touch_screen	MouseStatus	Master	Provides mouse events when the visualization window is in focus.
user_switches	ValueState	Slave	Provides state for the eight User DIP switches on the left side of the CLCD status bar, equivalent to switch S6 on VE hardware.

6.7.1.2 VEEVisualisation parameters

This section describes the configuration parameters.

The syntax to use in a configuration file or on the command line is:

```
motherboard.vis.<parameter>=<value>
```



Setting the `rate_limit-enable` parameter to `true` prevents the simulation from running too fast on fast workstations and enables timing loops and mouse actions to work correctly. However, it reduces the overall simulation speed. If your priority is high simulation speed, set `rate_limit-enable` to `false`, which is the default.

Table 6-14: VEEVisualisation parameters

Name	Type	Allowed values	Default value	Description
cluster0_name	string	-	Cluster0	Label for cluster 0 performance values.

Name	Type	Allowed values	Default value	Description
cluster1_name	string	-	Cluster1	Label for cluster 1 performance values.
cluster2_name	string	-	Cluster2	Label for cluster 2 performance values.
cluster3_name	string	-	Cluster3	Label for cluster 3 performance values.
cpu_name	string	-	-	Processor name displayed in window title.
daughter_led_count	int	0-32	0	Set to nonzero to display up to 32 LEDs. See the <code>daughter_leds</code> port.
daughter_user_switch_count	int	0-32	0	Set this parameter to display up to 32 switches. See the <code>daughter_user_switches</code> port.
diagnostics	bool	true, false	false	Print diagnostic messages.
disable_visualisation	bool	true, false	false	Disable the VESimulation component on model startup.
rate_limit-enable	bool	true, false	false	Restrict simulation speed so that simulation time more closely matches real time rather than running as fast as possible.
recorder.checkInstructionCount	bool	true, false	true	Check instruction count in recording file against actual instruction count during playback.
recorder.playbackFileName	string	-	""	Playback filename (empty string disables playback).
recorder.recordingFileName	string	-	""	Recording filename (empty string disables recording).
recorder.recordingTimeBase	int	-	0x5F5E100	Timebase in 1/s relative to the master clock, where 100000000 means 10 nanoseconds resolution simulated time for a 1 Hz master clock, for recording. Higher values give higher time resolution, playback timebase is always taken from the playback file.
recorder.verbose	int	-	0	Enable verbose messages (1=normal, 2=even more).
trap_key	int	Valid ATKeycode key value.	0x4A	Trap key that works with left Ctrl key to toggle mouse display. The default is the left Alt key, so press Left Alt and Left Ctrl simultaneously to toggle the mouse display.
window_title	string	-	"Fast Models - CLCD %cpu%"	Window title. <code>cpu_name</code> replaces <code>%cpu%</code> .

6.7.1.3 VESimulation verification and testing

This component passes tests by use as an I/O device for booting Linux and other operating systems.

6.7.1.4 VEVisualisation performance

Arm expects the elements in the status bar to have little effect on the performance of PV systems. However, applications that often redraw the contents of the frame buffer might incur overhead through GUI interactions on the host OS.

6.7.1.5 VEVisualisation library dependencies

This component relies on the Simple DirectMedia Layer (SDL) libraries, specifically `libSDL2-2.0.so.0.10.0`.

This library is bundled with Fast Models and is also available as an rpm for Red Hat Enterprise Linux. On Windows, the library is called `SDL2.dll`.

Related information

[Simple DirectMedia Layer \(SDL\) cross-platform development library](#)

6.8 VE_SysRegs component

This section describes the VE system registers component.

6.8.1 VE_SysRegs

This LISA+ component is a model of the VE status and system control registers.

6.8.2 VE_SysRegs ports

This table describes the VE_SysRegs ports.

Table 6-15: VE_SysRegs ports

Name	Protocol	Type	Description
<code>cb[0-1]</code>	<code>VECBProtocol</code>	Master	The Configuration Bus (CB) controls the power and reset sequence.
<code>clock_24Mhz</code>	<code>ClockSignal</code>	Slave	Reference clock for internal counter register.
<code>clock_100Hz</code>	<code>ClockSignal</code>	Slave	Reference clock for internal counter register.
<code>clock_CLCD</code>	<code>ClockRateControl</code>	Master	The clock for the LCD controller.
<code>lcd</code>	<code>LCD</code>	Master	Multimedia bus interface output to the LCD.
<code>leds</code>	<code>ValueState</code>	Master	Displays state of the <code>SYS_LED</code> register using the eight colored LEDs on the status bar.
<code>mmb[0-2]</code>	<code>LCD</code>	Slave	Multimedia bus interface input.
<code>mmc_card_present</code>	<code>StateSignal</code>	Slave	Indicates the presence of a MultiMedia Card (MMC) image.
<code>pvbuss</code>	<code>PVBus</code>	Slave	Slave port for connection to PV bus master/decoder.

Name	Protocol	Type	Description
system_reset	Signal	Master	Signal to the platform a complete system reset. Writes to the System Configuration registers can trigger the reset signal.
user_switches	ValueState	Master	Provides state for the eight User DIP switches on the left side of the CLCD status bar, equivalent to switch S6 on VE hardware.

6.8.3 VE_SysRegs parameters

This table describes the VE_SysRegs parameters.

Table 6-16: VE_SysRegs parameters

Name	Type	Default value	Description
exit_on_shutdown	bool	false	Used to shut down the system. See the Note after the table.
mmbSiteDefault	int	1	Default MultiMedia Bus (MMB) source (0=motherboard, 1=daughterboard 1, 2=daughterboard 2).
sys_proc_id0	int	0x0c000000	Processor ID register at CoreTile Express Site 1.
sys_proc_id1	int	0xff000000	Processor ID at CoreTile Express Site 2.
tilePresent	bool	true	Tile fitted.
user_switches_value	int	0	User switches.



When `exit_on_shutdown` is `true`, if software uses the `sys_cfgctrl` function `sys_cfg_shutdown`, then the simulator shuts down and exits. For more information on the `sys_cfgctrl` function values, see the Motherboard Express µATX V2M-P1 Technical Reference Manual.

6.8.4 VE_SysRegs registers

This table describes the configuration registers.

Table 6-17: VE_SysRegs registers

Name	Offset	Access	Description
SYS_ID	0x00	Read/write	System identity
SYS_SW	0x04	Read/write	Bits[7:0] map to switch S6
SYS_LED	0x08	Read/write	Bits[7:0] map to user LEDs
SYS_100HZ	0x24	Read only	100 Hz counter
SYS_FLAGS	0x30	Read/write	General purpose flags
SYS_FLAGSCLR	0x34	Write only	Clear bits in general purpose flags
SYS_NVFLAGS	0x38	Read/write	General purpose non-volatile flags
SYS_NVFLAGSCLR	0x3C	Write only	Clear bits in general purpose non-volatile flags
SYS_MCI	0x48	Read only	MCI
SYS_FLASH	0x4C	Read/write	Flash control

Name	Offset	Access	Description
SYS_CFGSW	0x58	Read/write	Boot select switch
SYS_24MHZ	0x5C	Read only	24 MHz counter
SYS_MISC	0x60	Read/write	Miscellaneous control flags
SYS_DMA	0x64	Read/write	DMA peripheral map
SYS_PROCID0	0x84	Read/write	Processor ID
SYS_PROCID1	0x88	Read/write	Processor ID
SYS_CFGDATA	0xA0	Read/write	Data to be read/written from/to motherboard controller
SYS_CFGCTRL	0xA4	Read/write	Control data transfer to motherboard controller
SYS_CFGSTAT	0xA8	Read/write	Status of data transfer to motherboard

6.8.5 VE_SysRegs - verification and testing

This component was tested as part of the Versatile™ Express model.

6.9 Differences between the VE hardware and the system models

This section describes features of the hardware that the models do not implement, or implement with significant differences.

6.9.1 Memory map

The model represents the memory map of the hardware VE platform, but is not an accurate representation of a specific revision.

The memory map in the supplied model is sufficiently complete and accurate to boot the same operating system images as for the VE hardware.

In the memory map, memory regions that are not explicitly occupied by a peripheral or by memory are unmapped. This includes regions otherwise occupied by a peripheral that is not implemented, and those areas that are documented as reserved. Accessing these regions from the host processor results in the model presenting a warning.

6.9.2 Memory aliasing

The model implements address-space aliasing of the DRAM. This means that the same physical memory locations are visible at different addresses.

The lower 2 GB of the DRAM is accessible at 0x00_80000000. The full 4 GB of DRAM is accessible at 0x08_00000000 and again at 0x80_00000000. The aliasing of DRAM then repeats from 0x81_00000000 up to 0xFF_FFFFFFFF.

6.9.3 VE hardware features absent

These FVPs do not implement the following features of the hardware:

- Two-wire serial bus interfaces.
- USB interfaces.
- PCI Express interfaces.
- Compact flash.
- Digital Visual Interface (DVI).
- Debug and test interfaces.
- Dynamic Memory Controller (DMC).
- Static Memory Controller (SMC).

Related information

[VE memory map for Cortex-A_series](#) on page 170

6.9.4 VE hardware features different

These Fixed Virtual Platforms only partially implement some features of the hardware.

The partially implemented features might not work as you expect. Check the model release notes for the latest information.

Sound

The VE FVPs implement the PL041 AACI PrimeCell and the audio CODEC as in the VE hardware, but with a limited number of sample rates.

6.10 VE Platform FVPs

This section lists the instances in each FVP.

6.10.1 Instances for FVP_VE_Cortex-R4

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R4](#)
- [AudioOut_SDL](#)
- [ClockDivider](#)
- [ClockTimerThread](#)

- [ClockTimerThread64](#)
- [CounterModule](#)
- [FVP_VE_Cortex_R4](#)
- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [MMC](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL310_L2CC](#)
- [PL390_GIC](#)
- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVCache](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TelnetTerminal](#)
- [VEDaughterBoardCortex_R4](#)
- [VEInterruptMapper](#)
- [VEMotherBoardR](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)

- [VisEventRecorder](#)
- [WarningMemory](#)

6.10.2 Instances for FVP_VE_Cortex-R5x1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R5](#)
- [AudioOut_SDL](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R5](#)
- [CounterModule](#)
- [FVP_VE_Cortex_R5x1](#)
- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [MMC](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)
- [PL11x_CLCD](#)
- [PL180_MCI](#)
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- [PS2Keyboard](#)
- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)

- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TelnetTerminal](#)
- [VEDaughterBoardCortex_R5x1](#)
- [VEInterruptMapper](#)
- [VEMotherBoardR](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VisEventRecorder](#)
- [WarningMemory](#)

6.10.3 Instances for FVP_VE_Cortex-R7x1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R7](#)
- [AudioOut_SDL](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R7](#)
- [CounterModule](#)
- [FVP_VE_Cortex_R7x1](#)
- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [MMC](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
- [PL050_KMI](#)
- [PL111_CLCD](#)

- [PL11x_CLCD](#)
- [PL180_MCI](#)
- [PL310_L2CC](#)
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- [PS2Mouse](#)
- [PVBusExclusiveMonitor](#)
- [PVCache](#)
- [RAMDevice](#)
- [SMSC_91C111](#)
- [SP804_Timer](#)
- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TelnetTerminal](#)
- [VEDaughterBoardCortex_R7x1](#)
- [VEInterruptMapper](#)
- [VEMotherBoardR](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VisEventRecorder](#)
- [WarningMemory](#)

6.10.4 Instances for FVP_VE_Cortex-R8x1

This FVP contains the following instances. For components that are supplied in Fast Models, there are links to the Fast Models Reference Guide.

- [ARM_Cortex-R8](#)
- [AudioOut_SDL](#)
- [ClockDivider](#)
- [ClockTimerThread](#)
- [ClockTimerThread64](#)
- [Cluster_ARM_Cortex-R8](#)
- [CounterModule](#)
- [FVP_VE_Cortex_R8x1](#)

- [FlashLoader](#)
- [GUIPoll](#)
- [HostBridge](#)
- [IntelStrataFlashJ3](#)
- [MMC](#)
- [PL011_Uart](#)
- [PL031_RTC](#)
- [PL041_AACI](#)
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- [SP805_Watchdog](#)
- [SP810_SysCtrl](#)
- [SchedulerThread](#)
- [SchedulerThreadEvent](#)
- [TelnetTerminal](#)
- [VEDaughterBoardCortex_R8x1](#)
- [VEInterruptMapper](#)
- [VEMotherBoardR](#)
- [VEVisualisation](#)
- [VE_SysRegs](#)
- [VisEventRecorder](#)
- [WarningMemory](#)

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Product and document information

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Product status

All products and services provided by Arm require deliverables to be prepared and made available at different levels of completeness. The information in this document indicates the appropriate level of completeness for the associated deliverables.

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Revision history

These sections can help you understand how the document has changed over time.

Document release information

The Document history table gives the issue number and the released date for each released issue of this document.

Document history

Issue	Date	Confidentiality	Change
1130-00	19 November 2025	Non-Confidential	Update for v11.30
1129-00	16 May 2025	Non-Confidential	New document for v11.29

Change history

For technical changes to this documentation, see the [Fast Models Release Notes](#).

Conventions

The following subsections describe conventions used in Arm documents.

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The Arm Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

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Convention	Use
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bold	Interface elements, such as menu names. Terms in descriptive lists, where appropriate.
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monospace <u>underline</u>	A permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: <div>MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2></div>
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